

## easySPIN – fully integrated microstepping motor driver

Datasheet – production data

### Features

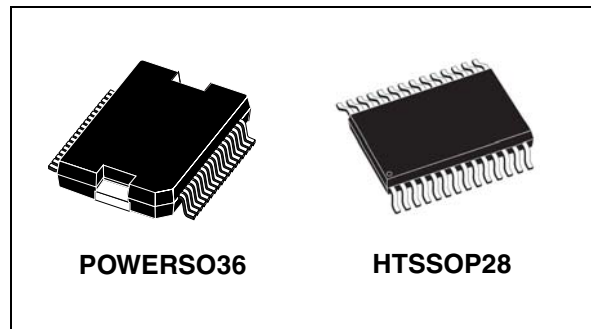
- Operating voltage: 8 - 45 V
- 7.0 A output peak current (3.0 A r.m.s.)
- Low  $R_{DS(on)}$  Power MOSFETs
- Programmable power MOS slew-rate
- Up to 1/16 microstepping
- Current control with adaptive decay
- Non-dissipative current sensing
- SPI interface
- Low quiescent and standby currents
- Programmable non-dissipative overcurrent protection on all power MOS
- Two-level overtemperature protection

### Applications

- Bipolar stepper motor

### Description

The L6474, realized in analog mixed signal technology, integrates a dual low  $R_{DS(on)}$  DMOS full-bridge with all power switches equipped with an accurate on-chip current sensing circuitry suitable for non-dissipative current control and overcurrent protections. Thanks to a new current control, a 1/16 microstepping is achieved through



an adaptive decay mode which outperforms traditional implementations.

All data registers, including those used to set analogue values (i.e. current control value, current protection trip point, dead time, etc.) are sent through a standard 5 Mbit/s SPI.

A very rich set of protections (thermal, low bus voltage, overcurrent) makes the L6474 “bullet proof” as required by the most demanding motor control applications.

**Table 1. Device summary**

Order code	Package	Packing
L6474H	HTSSOP28	Tube
L6474HTR	HTSSOP28	Tape and reel
L6474PD	POWERSO36	Tube
L6474PDTR	POWERSO36	Tape and reel

# Contents

- 1      Block diagram ..... 7**
- 2      Electrical data ..... 8**
  - 2.1 Absolute maximum ratings ..... 8
  - 2.2 Recommended operating conditions ..... 9
  - 2.3 Thermal data ..... 9
- 3      Electrical characteristics ..... 10**
- 4      Pin connection ..... 15**
  - 4.1 Pin list ..... 16
- 5      Typical applications ..... 18**
- 6      Functional description ..... 19**
  - 6.1 Device power-up ..... 19
  - 6.2 Logic I/O ..... 19
  - 6.3 Charge pump ..... 19
  - 6.4 Microstepping ..... 20
  - 6.5 Absolute position counter ..... 21
  - 6.6 Step sequence control ..... 21
  - 6.7 Enable and disable commands ..... 21
  - 6.8 Internal oscillator and oscillator driver ..... 22
    - 6.8.1 Internal oscillator ..... 22
    - 6.8.2 External clock source ..... 22
  - 6.9 Overcurrent detection ..... 23
  - 6.10 Undervoltage lock-out (UVLO) ..... 24
  - 6.11 Thermal warning and thermal shutdown ..... 24
  - 6.12 Reset and standby ..... 24
  - 6.13 Programmable DMOS slew-rate, dead-time and blanking-time ..... 25
  - 6.14 Integrated analog to digital converter ..... 25
  - 6.15 Internal voltage regulator ..... 25

6.16	SYNC pin	26
6.17	FLAG pin	26
<b>7</b>	<b>Phase current control</b>	<b>27</b>
7.1	Peak current control	27
7.2	Auto-adjusted decay mode	28
7.3	Auto-adjusted fast decay during the falling steps	29
7.4	Torque regulation (output current amplitude regulation)	30
<b>8</b>	<b>Serial interface</b>	<b>31</b>
<b>9</b>	<b>Programming manual</b>	<b>33</b>
9.1	Registers and flags description	33
9.1.1	ABS_POS	34
9.1.2	EL_POS	34
9.1.3	MARK	34
9.1.4	TVAL	34
9.1.5	T_FAST	35
9.1.6	TON_MIN	35
9.1.7	TOFF_MIN	36
9.1.8	ADC_OUT	37
9.1.9	OCD_TH	37
9.1.10	STEP_MODE	38
9.1.11	ALARM_EN	40
9.1.12	CONFIG	40
9.1.13	STATUS	42
9.2	Application commands	43
9.2.1	Command management	43
9.2.2	Nop	44
9.2.3	SetParam (PARAM, VALUE)	45
9.2.4	GetParam (PARAM)	45
9.2.5	Enable	46
9.2.6	Disable	46
9.2.7	GetStatus	46
<b>10</b>	<b>Package mechanical data</b>	<b>47</b>

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**11      Revision history ..... 51**

## List of tables

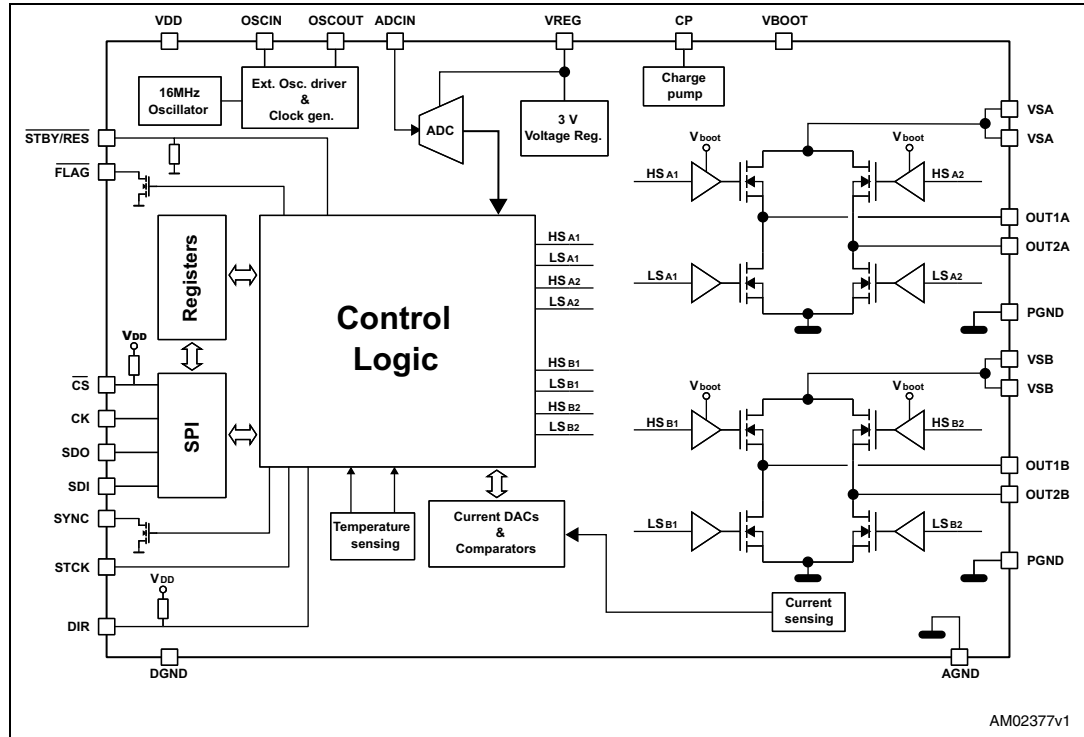
Table 1.	Device summary . . . . .	1
Table 2.	Absolute maximum ratings . . . . .	8
Table 3.	Recommended operating conditions . . . . .	9
Table 4.	Thermal data . . . . .	9
Table 5.	Electrical characteristics . . . . .	10
Table 6.	Pin description . . . . .	16
Table 7.	Typical application values . . . . .	18
Table 8.	CL values according to external oscillator frequency . . . . .	22
Table 9.	Register map . . . . .	33
Table 10.	EL_POS register . . . . .	34
Table 11.	Torque regulation register . . . . .	35
Table 12.	T_FAST register . . . . .	35
Table 13.	Maximum fast decay times . . . . .	35
Table 14.	Minimum ON time . . . . .	36
Table 15.	Minimum OFF time . . . . .	36
Table 16.	ADC_OUT value and torque regulation feature . . . . .	37
Table 17.	Overcurrent detection threshold . . . . .	37
Table 18.	STEP_MODE register . . . . .	38
Table 19.	Step mode selection . . . . .	38
Table 20.	SYNC signal source . . . . .	39
Table 21.	ALARM_EN register . . . . .	40
Table 22.	CONFIG register . . . . .	40
Table 23.	Oscillator management . . . . .	41
Table 24.	Overcurrent event . . . . .	41
Table 25.	Programmable power bridge output slew-rate values . . . . .	42
Table 26.	External torque regulation enable . . . . .	42
Table 27.	OFF time . . . . .	42
Table 28.	STATUS register . . . . .	42
Table 29.	STATUS register DIR bit . . . . .	43
Table 30.	Application commands . . . . .	43
Table 31.	Nop command structure . . . . .	44
Table 32.	SetParam command structure . . . . .	45
Table 33.	GetParam command structure . . . . .	45
Table 34.	HardStop command structure . . . . .	46
Table 35.	Disable command structure . . . . .	46
Table 36.	GetStatus command structure . . . . .	46
Table 37.	HTSSOP28 mechanical data . . . . .	47
Table 38.	POWERSO36 mechanical data . . . . .	49
Table 39.	Document revision history . . . . .	51

## List of figures

Figure 1.	Block diagram . . . . .	7
Figure 2.	HTSSOP28 pin connection (top view) . . . . .	15
Figure 3.	POWERSO36 pin connection (top view) . . . . .	15
Figure 4.	Bipolar stepper motor control application using L6474 . . . . .	18
Figure 5.	Charge pump circuitry . . . . .	20
Figure 6.	Normal mode and microstepping (16 microsteps) . . . . .	20
Figure 7.	OSCIN and OSCOUT pin configurations . . . . .	23
Figure 8.	Internal 3 V linear regulator . . . . .	25
Figure 9.	Peak current control . . . . .	27
Figure 10.	Adaptive decay - fast decay tuning . . . . .	28
Figure 11.	Adaptive decay - switch from normal to slow+fast decay mode and vice versa . . . . .	29
Figure 12.	Fast decay tuning during the falling steps . . . . .	30
Figure 13.	SPI timings diagram . . . . .	31
Figure 14.	Daisy-chain configuration . . . . .	32
Figure 15.	Command with three-byte argument . . . . .	44
Figure 16.	Command with three-byte response . . . . .	44
Figure 17.	Command response aborted . . . . .	44
Figure 18.	HTSSOP28 mechanical data . . . . .	48
Figure 19.	POWERSO36 drawings . . . . .	50

# 1 Block diagram

Figure 1. Block diagram



## 2 Electrical data

### 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Test condition	Value	Unit
$V_{DD}$	Logic interface supply voltage		5.5	V
$V_S$	Motor supply voltage	$V_{SA} = V_{SB} = V_S$	48	V
$V_{GND, diff}$	Differential voltage between AGND, PGND and DGND		$\pm 0.3$	V
$V_{boot}$	Bootstrap peak voltage		55	V
$V_{REG}$	Internal voltage regulator output pin and logic supply voltage		3.6	V
$V_{ADCIN}$	Integrated ADC input voltage range (ADCIN pin)		-0.3 to +3.6	V
$V_{OSC}$	OSCIN and OSCOUT pin voltage range		-0.3 to +3.6	V
$V_{out\_diff}$	Differential voltage between $V_{SA}$ , OUT1 <sub>A</sub> , OUT2 <sub>A</sub> , PGND and $V_{SB}$ , OUT1 <sub>B</sub> , OUT2 <sub>B</sub> , PGND pins	$V_{SA} = V_{SB} = V_S$	48	V
$V_{LOGIC}$	Logic inputs voltage range		-0.3 to +5.5	V
$I_{out}^{(1)}$	R.m.s. output current		3	A
$I_{out\_peak}^{(1)}$	Pulsed output current	$T_{PULSE} < 1 \text{ ms}$	7	A
$T_{OP}$	Operating junction temperature		-40 to 150	°C
$T_S$	Storage temperature range		-55 to 150	°C
$P_{tot}$	Total power dissipation ( $T_A = 25 \text{ °C}$ ) <sup>(2)</sup>		5	W

1. Maximum output current limit is related to metal connection and bonding characteristics. Actual limit must satisfy maximum thermal dissipation constraints.

2. HTSSOP28 mounted on EVAL6474H.



## 2.2 Recommended operating conditions

**Table 3. Recommended operating conditions**

Symbol	Parameter	Test condition	Value		Unit
V <sub>DD</sub>	Logic interface supply voltage	3.3 V logic outputs		3.3	V
		5 V logic outputs		5	
V <sub>S</sub>	Motor supply voltage	V <sub>SA</sub> = V <sub>SB</sub> = V <sub>S</sub>	8	45	V
V <sub>out_diff</sub>	Differential voltage between V <sub>SA</sub> , OUT1 <sub>A</sub> , OUT2 <sub>A</sub> , PGND and V <sub>SB</sub> , OUT1 <sub>B</sub> , OUT2 <sub>B</sub> , PGND pins	V <sub>SA</sub> = V <sub>SB</sub> = V <sub>S</sub>		45	V
V <sub>REG,in</sub>	Logic supply voltage	V <sub>REG</sub> voltage imposed by external source	3.2	3.3	V
V <sub>ADC</sub>	Integrated ADC input voltage (ADCIN pin)		0	V <sub>REG</sub>	V

## 2.3 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Package	Typ.	Unit
R <sub>thJA</sub>	Thermal resistance junction-ambient	HTSSOP28 <sup>(1)</sup>	22	°C/W
		POWERSO36 <sup>(2)</sup>	12	

1. HTSSOP28 mounted on EVAL6474H Rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 cm<sup>2</sup> on each layer and 15 via holes below the IC.
2. POWERSO36 mounted on EVAL6474PD Rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 cm<sup>2</sup> on each layer and 22 via holes below the IC.

### 3 Electrical characteristics

$V_{SA} = V_{SB} = 36\text{ V}$ ;  $V_{DD} = 3.3\text{ V}$ ; internal 3 V regulator;  $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 5. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>General</b>						
$V_{SthOn}$	$V_S$ UVLO turn-on threshold		7.5	8.2	8.9	V
$V_{SthOff}$	$V_S$ UVLO turn-off threshold		6.6	7.2	7.8	V
$V_{SthHyst}$	$V_S$ UVLO threshold hysteresis		0.7	1	1.3	V
$I_q$	Quiescent motor supply current	Internal oscillator selected; $V_{REG} = 3.3\text{ V}$ ext; CP floating		0.5	0.65	mA
$T_{j(WRN)}$	Thermal warning temperature			130		$^\circ\text{C}$
$T_{j(SD)}$	Thermal shutdown temperature			160		$^\circ\text{C}$
<b>Charge pump</b>						
$V_{pump}$	Voltage swing for charge pump oscillator			10		V
$f_{pump,min}$	Minimum charge pump oscillator frequency (1)			660		kHz
$f_{pump,max}$	Maximum charge pump oscillator frequency (1)			800		kHz
$I_{boot}$	Average boot current	$f_{sw,A} = f_{sw,B} = 15.6\text{ kHz}$ $POW\_SR = '10'$		1.1	1.4	mA
<b>Output DMOS transistor</b>						
$R_{DS(on)}$	High-side switch ON resistance	$T_J = 25\text{ }^\circ\text{C}$ , $I_{out} = 3\text{ A}$		0.37		$\Omega$
		$T_J = 125\text{ }^\circ\text{C}$ , (2) $I_{out} = 3\text{ A}$		0.51		
	Low-side switch ON resistance	$T_J = 25\text{ }^\circ\text{C}$ , $I_{out} = 3\text{ A}$		0.18		
		$T_J = 125\text{ }^\circ\text{C}$ , (2) $I_{out} = 3\text{ A}$		0.23		
$I_{DSS}$	Leakage current	OUT = $V_S$			3.1	mA
		OUT = GND	-0.3			
$t_r$	Rise time (3)	$POW\_SR = '00'$ , $I_{out} = +1\text{ A}$		100		ns
		$POW\_SR = '00'$ , $I_{out} = -1\text{ A}$		80		
		$POW\_SR = '11'$ , $I_{out} = \pm 1\text{ A}$		100		
		$POW\_SR = '10'$ , $I_{out} = \pm 1\text{ A}$		200		
		$POW\_SR = '01'$ , $I_{out} = \pm 1\text{ A}$		300		

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_f$	Fall time <sup>(3)</sup>	POW_SR = '00', $I_{out} = +1A$		90		ns
		POW_SR = '00', $I_{out} = -1A$		110		
		POW_SR = '11', $I_{out} = \pm 1A$		110		
		POW_SR = '10', $I_{out} = \pm 1A$		260		
		POW_SR = '01', $I_{load} = \pm 1A$		375		
$SR_{out,r}$	Output rising slew-rate	POW_SR = '00', $I_{out} = +1A$		285		V/ $\mu$ s
		POW_SR = '00', $I_{out} = -1A$		360		
		POW_SR = '11', $I_{out} = \pm 1A$		285		
		POW_SR = '10', $I_{out} = \pm 1A$		150		
		POW_SR = '01', $I_{out} = \pm 1A$		95		
$SR_{out,f}$	Output falling slew-rate	POW_SR = '00', $I_{out} = +1A$		320		V/ $\mu$ s
		POW_SR = '00', $I_{out} = -1A$		260		
		POW_SR = '11', $I_{out} = \pm 1A$		260		
		POW_SR = '10', $I_{out} = \pm 1A$		110		
		POW_SR = '01', $I_{out} = \pm 1A$		75		
<b>Dead time and blanking</b>						
$t_{DT}$	Dead time <sup>(1)</sup>	POW_SR = '00'		250		ns
		POW_SR = '11', $f_{OSC} = 16$ MHz		375		
		POW_SR = '10', $f_{OSC} = 16$ MHz		625		
		POW_SR = '01', $f_{OSC} = 16$ MHz		875		
$t_{blank}$	Blanking time <sup>(1)</sup>	POW_SR = '00'		250		ns
		POW_SR = '11', $f_{OSC} = 16$ MHz		375		
		POW_SR = '10', $f_{OSC} = 16$ MHz		625		
		POW_SR = '01', $f_{OSC} = 16$ MHz		875		
<b>Source-drain diodes</b>						
$V_{SD,HS}$	High-side diode forward ON voltage	$I_{out} = 1$ A		1	1.1	V
$V_{SD,LS}$	Low-side diode forward ON voltage	$I_{out} = 1$ A		1	1.1	V
$t_{rrHS}$	High-side diode reverse recovery time	$I_{out} = 1$ A		30		ns
$t_{rrLS}$	Low-side diode reverse recovery time	$I_{out} = 1$ A		100		ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Logic inputs and outputs</b>						
$V_{IL}$	Low logic level input voltage				0.8	V
$V_{IH}$	High logic level input voltage		2			V
$I_{IH}$	High logic level input current <sup>(4)</sup>	$V_{IN} = 5\text{ V}$			1	$\mu\text{A}$
$I_{IL}$	Low logic level input current <sup>(5)</sup>	$V_{IN} = 0\text{ V}$	-1			$\mu\text{A}$
$V_{OL}$	Low logic level output voltage <sup>(6)</sup>	$V_{DD} = 3.3\text{ V}, I_{OL} = 4\text{ mA}$			0.3	V
		$V_{DD} = 5\text{ V}, I_{OL} = 4\text{ mA}$			0.3	
$V_{OH}$	High logic level output voltage	$V_{DD} = 3.3\text{ V}, I_{OH} = 4\text{ mA}$	2.4			V
		$V_{DD} = 5\text{ V}, I_{OH} = 4\text{ mA}$	4.7			
$R_{PU}$ $R_{PD}$	CS pull-up and STBY pull-down resistors	$\overline{CS} = \text{GND};$ $\text{STBY}/\text{RST} = 5\text{ V}$	335	430	565	$\text{k}\Omega$
$R_{PUDIR}$	DIR input pull-up resistance	DIR = GND	60	85	110	$\text{k}\Omega$
$I_{logic}$	Internal logic supply current	3.3 V $V_{REG}$ externally supplied, internal oscillator		3.7	4.3	mA
$I_{logic,STBY}$	Standby mode internal logic supply current	3.3 V $V_{REG}$ externally supplied		2	2.5	$\mu\text{A}$
$f_{STCK}$	Step clock input frequency				2	MHz
<b>Internal oscillator and external oscillator driver</b>						
$f_{osc,i}$	Internal oscillator frequency	$T_J = 25\text{ }^\circ\text{C}, V_{REG} = 3.3\text{ V}$	-3%	16	+3%	MHz
$f_{osc,e}$	Programmable external oscillator frequency		8		32	MHz
$V_{OSCOUTH}$	OSCOUT clock source high level voltage	Internal oscillator 3.3 V $V_{REG}$ externally supplied; $I_{OSCOUT} = 4\text{ mA}$	2.4			V
$V_{OSCOU TL}$	OSCOUT clock source low level voltage	Internal oscillator 3.3 V $V_{REG}$ externally supplied; $I_{OSCOUT} = 4\text{ mA}$			0.3	V
$t_{rOSCOUT}$ $t_{fOSCOUT}$	OSCOUT clock source rise and fall time	Internal oscillator			20	ns
$t_{extosc}$	Internal to external oscillator switching delay			3		ms
$t_{intosc}$	External to internal oscillator switching delay			1.5		$\mu\text{s}$
<b>SPI</b>						
$f_{CK,MAX}$	Maximum SPI clock frequency <sup>(7)</sup>		5			MHz
$t_{rCK}$ $t_{fCK}$	SPI clock rise and fall time <sup>(7)</sup>	$C_L = 30\text{ pF}$			25	ns
$t_{hCK}$ $t_{lCK}$	SPI clock high and low time <sup>(7)</sup>		75			ns
$t_{setCS}$	Chip select set-up time <sup>(7)</sup>		350			ns
$t_{holCS}$	Chip select hold time <sup>(7)</sup>		10			ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{disCS}$	Deselect time <sup>(7)</sup>		800			ns
$t_{setSDI}$	Data input set-up time <sup>(7)</sup>		25			ns
$t_{holSDI}$	Data input hold time <sup>(7)</sup>		20			ns
$t_{enSDO}$	Data output enable time <sup>(7)</sup>				38	ns
$t_{disSDO}$	Data output disable time <sup>(7)</sup>				47	ns
$t_{vSDO}$	Data output valid time <sup>(7)</sup>				57	ns
$t_{holSDO}$	Data output hold time <sup>(7)</sup>		37			ns
<b>Current control</b>						
$I_{STEP,max}$	Max. programmable reference current			4		A
$I_{STEP,min}$	Min. programmable reference current			31		mA
<b>Overcurrent protection</b>						
$I_{OCD,MAX}$	Maximum programmable overcurrent detection threshold	OCD_TH = '1111'		6		A
$I_{OCD,MIN}$	Minimum programmable overcurrent detection threshold	OCD_TH = '0000'		0.375		A
$I_{OCD,RES}$	Programmable overcurrent detection threshold resolution			0.375		A
$t_{OCD,Flag}$	OCD to flag signal delay time	$dl_{out}/dt = 350A/\mu s$		650	1000	ns
$t_{OCD,SD}$	OCD to shut down delay time	$dl_{out}/dt = 350A/\mu s$ POW_SR = '10'		600		$\mu s$
<b>Standby</b>						
$I_{qSTBY}$	Quiescent motor supply current in standby conditions	$V_S = 8 V$		26	34	$\mu A$
		$V_S = 36 V$		30	36	
$t_{STBY,min}$	Minimum standby time			10		$\mu s$
$t_{logicwu}$	Logic power-on and wake-up time			38	45	$\mu s$
$t_{cpwu}$	Charge pump power-on and wake-up time	Power bridges disabled, $C_p = 10 nF$ , $C_{boot} = 220 nF$		650		$\mu s$
<b>Internal voltage regulator</b>						
$V_{REG}$	Voltage regulator output voltage		2.9	3	3.2	V
$I_{REG}$	Voltage regulator output current				40	mA
$V_{REG,drop}$	Voltage regulator output voltage drop	$I_{REG} = 40 mA$		50		mV
$I_{REG,STBY}$	Voltage regulator standby output current				10	mA
<b>Integrated analog to digital converter</b>						
$N_{ADC}$	Analog to digital converter resolution			5		bit

**Table 5. Electrical characteristics (continued)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{\text{ADC,ref}}$	Analog to digital converter reference voltage			$V_{\text{REG}}$		V
$f_{\text{S}}$	Analog to digital converter sampling frequency			$f_{\text{OSC}}/512$		kHz

1. Accuracy depends on oscillator frequency accuracy.
2. Tested at 25 °C in a restricted range and guaranteed by characterization.
3. Rise and fall time depends on motor supply voltage value. Refer to  $SR_{\text{out}}$  values ([Table 5](#)) in order to evaluate the actual rise and fall time.
4. Not valid for  $\overline{\text{STBY/RST}}$  pins which have internal pull-down resistor.
5. Not valid for SW and CS pins which have internal pull-up resistor.
6.  $\overline{\text{FLAG}}$  and SYNC open drain outputs included.
7. See [Figure 13](#)– SPI timings diagram for details.

# 4 Pin connection

Figure 2. HTSSOP28 pin connection (top view)

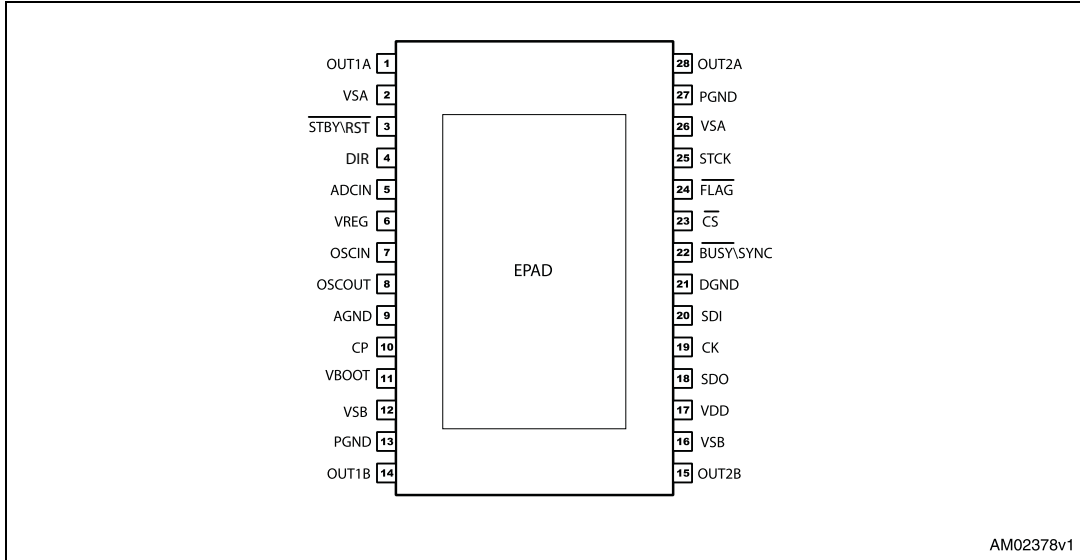
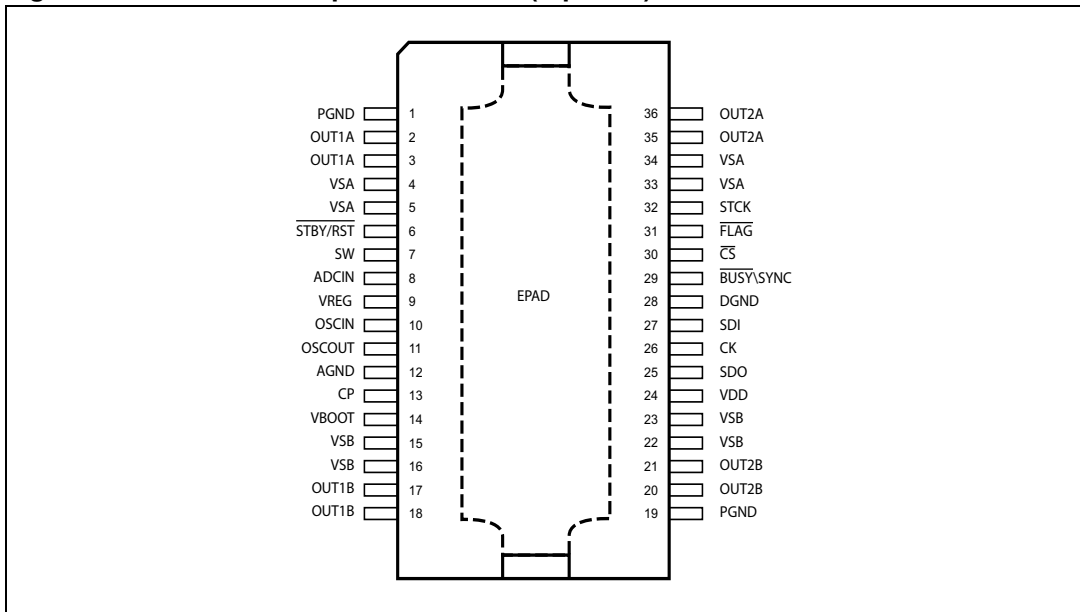


Figure 3. POWERSO36 pin connection (top view)



## 4.1 Pin list

**Table 6. Pin description**

N.	Name	Type	Function
17	VDD	Power	Logic outputs supply voltage (pull-up reference)
6	VREG	Power	Internal 3 V voltage regulator output and 3.3 V external logic supply
7	OSCIN	Analog input	Oscillator pin 1. To connect an external oscillator or clock source. If this pin is unused, it should be left floating.
8	OSCOUT	Analog output	Oscillator pin 2. To connect an external oscillator. When the internal oscillator is used this pin can supply 2/4/8/16 MHz. If this pin is unused, it should be left floating.
10	CP	Output	Charge pump oscillator output
11	VBOOT	Supply voltage	Bootstrap voltage needed for driving the high-side power DMOS of both bridges (A and B)
5	ADCIN	Analog input	Internal analog to digital converter input
2 26	VSA	Power supply	Full-bridge A power supply pin. It must be connected to VSB
12 16	VSB	Power supply	Full-bridge B power supply pin. It must be connected to VSA
27 13	PGND	Ground	Power ground pin
1	OUT1A	Power output	Full-bridge A output 1
28	OUT2A	Power output	Full-bridge A output 2
14	OUT1B	Power output	Full-bridge B output 1
15	OUT2B	Power output	Full-bridge B output 2
9	AGND	Ground	Analog ground
4	DIR	Logical input	Direction input
21	DGND	Ground	Digital ground
22	SYNC	Open drain output	Synchronization signal.
18	SDO	Logic output	Data output pin for serial interface
20	SDI	Logic input	Data input pin for serial interface
19	CK	Logic input	Serial interface clock
23	$\overline{CS}$	Logic input	Chip select input pin for serial interface
24	$\overline{FLAG}$	Open drain output	Status flag pin. An internal open drain transistor can pull the pin to GND when a programmed alarm condition occurs (step loss, OCD, thermal pre-warning or shutdown, UVLO, wrong command, non performable command)
3	$\overline{STBY/RST}$	Logic input	Standby and reset pin. LOW logic level resets the logic and puts the device into standby mode. If not used, should be connected to VDD



**Table 6. Pin description (continued)**

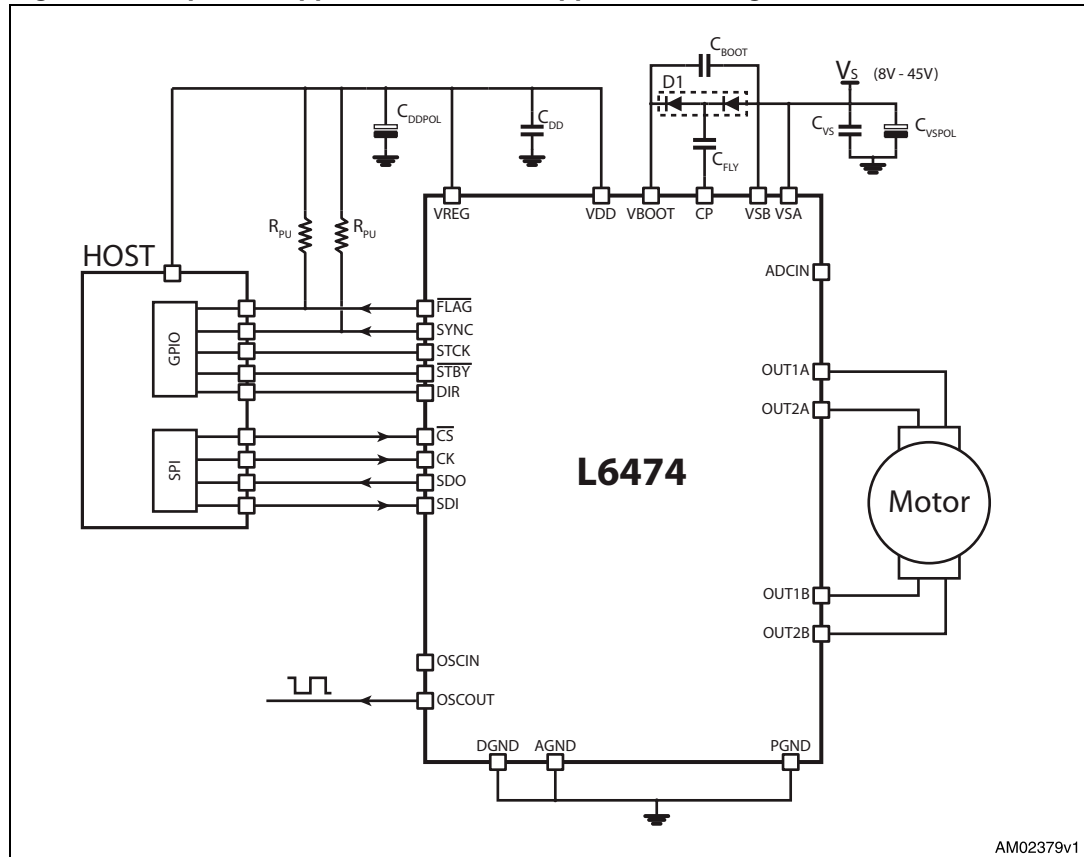
<b>N.</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
25	STCK	Logic input	Step clock input
EPAD	Exposed pad	Ground	Internally connected to PGND, AGND and DGND pins

## 5 Typical applications

Table 7. Typical application values

Name	Value
$C_{VS}$	220 nF
$C_{VSPOL}$	100 $\mu$ F
$C_{REG}$	100 nF
$C_{REGPOL}$	47 $\mu$ F
$C_{DD}$	100 nF
$C_{DDPOL}$	10 $\mu$ F
D1	Charge pump diodes
$C_{BOOT}$	220 nF
$C_{FLY}$	10 nF
$R_{PU}$	39 k $\Omega$
$R_{SW}$	100 $\Omega$
$C_{SW}$	10 nF

Figure 4. Bipolar stepper motor control application using L6474



## 6 Functional description

### 6.1 Device power-up

At power-up end, the device state is the following:

- Registers are set to default
- Internal logic is driven by internal oscillator and a 2 MHz clock is provided by the OSCOUT pin
- Bridges are disabled (High Z)
- UVLO bit in STATUS register is forced low (fail condition)
- FLAG output is forced low.

During power-up the device is under reset (all logic IO disabled and power bridges in high impedance state) until the following conditions are satisfied:

- $V_S$  is greater than  $V_{SthOn}$
- $V_{REG}$  is greater than  $V_{REGth} = 2.8\text{ V}$  typical
- Internal oscillator is operative.

### 6.2 Logic I/O

Pins  $\overline{CS}$ , CK, SDI, STCK, DIR and  $\overline{STBY}\overline{RST}$  are TTL/CMOS 3.3 V-5 V compatible logic inputs.

Pin SDO is a TTL/CMOS compatible logic output. VDD pin voltage sets the logic output pin voltage range; when it is connected to VREG or 3.3 V external supply voltage, the output is 3.3 V compatible. When VDD is connected to a 5 V supply voltage, SDO is 5 V compatible.

VDD is not internally connected to  $V_{REG}$ , an external connection is always needed.

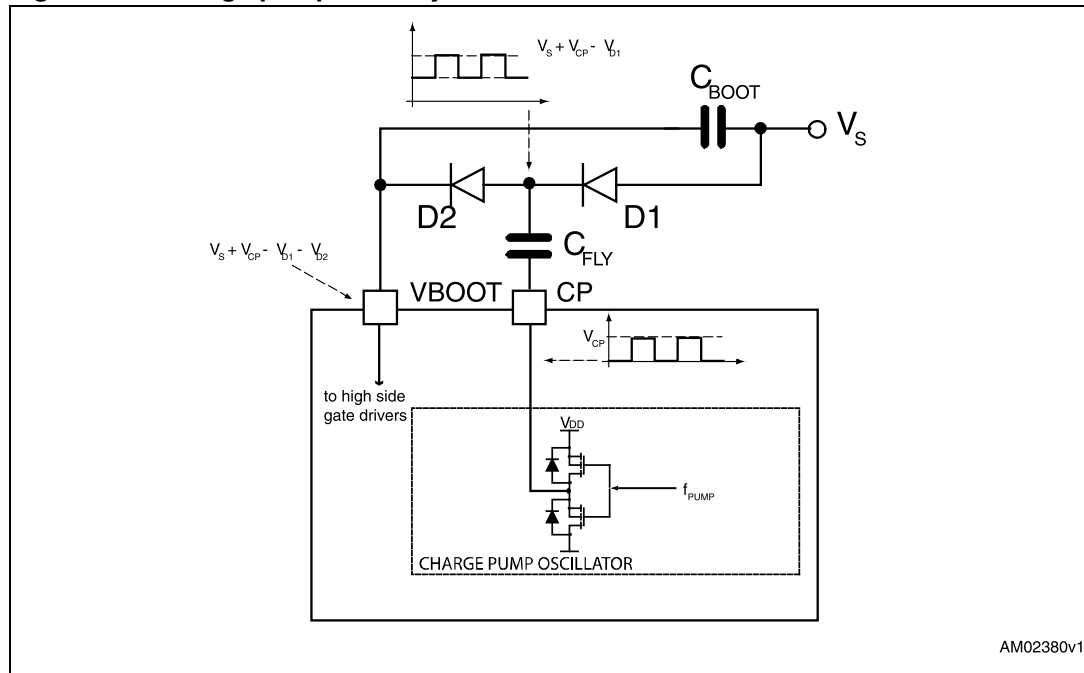
A 10  $\mu\text{F}$  capacitor should be connected to the VDD pin in order to obtain a proper operation.

Pins  $\overline{FLAG}$  and SYNC are open drain outputs.

### 6.3 Charge pump

To ensure the correct driving of the high-side integrated MOSFETs, a voltage higher than the motor power supply voltage needs to be applied to the VBOOT pin. The high-side gate driver supply voltage VBOOT is obtained through an oscillator and a few external components realizing a charge pump (see [Figure 5](#)).

Figure 5. Charge pump circuitry

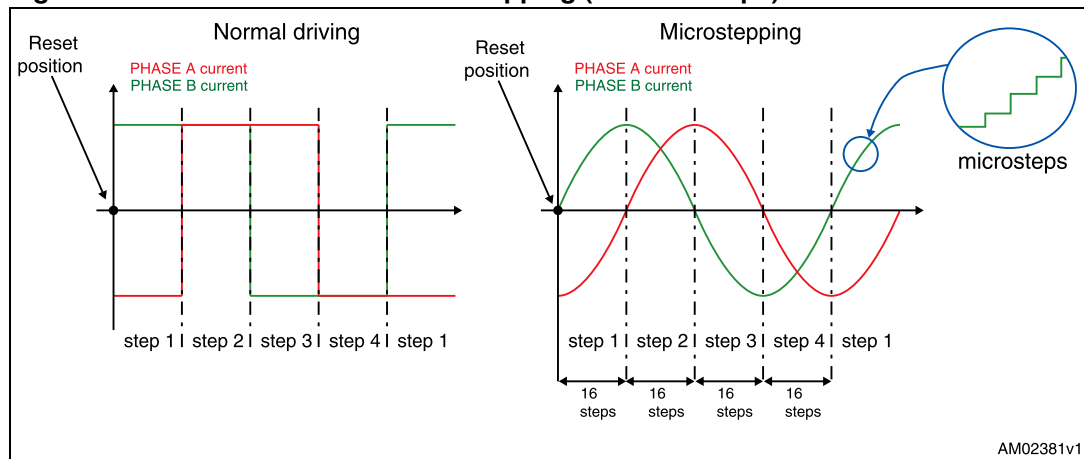


## 6.4 Microstepping

The driver is able to divide the single step into up to 16 microsteps. Stepping mode can be programmed by STEP\_SEL parameter in STEP\_MODE register (see [Table 19](#)).

Step mode can only be changed when bridges are disabled. Every time the step mode is changed, the electrical position (i.e. the point of microstepping sinewave that is generated) is reset to the first microstep and the absolute position counter value (see [Section 6.5](#)) becomes meaningless.

Figure 6. Normal mode and microstepping (16 microsteps)



## 6.5 Absolute position counter

An internal 22 bit register (ABS\_POS) takes memory of motor motion according to the selected step mode; the stored value unit is equal to the selected step mode (full, half, quarter, etc.). The position range is from  $-2^{21}$  to  $+2^{21}-1$  ( $\mu$ ) steps (see [Section 9.1.1](#)).

## 6.6 Step sequence control

The motor movement is defined by the step clock signal applied to the STCK pin. At each step clock rising edge, the motor is moved by one microstep in the direction selected by DIR input (high for forward direction and low for reverse direction) and absolute position is consequently updated.

## 6.7 Enable and disable commands

The power stage of the device can be enabled and disabled through the respective SPI commands.

The enable command turns on the power outputs and starts the current control algorithm. The phase currents are controlled according to present EL\_POS value. If a fault condition requires the power stage to be disabled, the command is ignored.

The disable command immediately forces the power outputs in a high impedance condition.

## 6.8 Internal oscillator and oscillator driver

The control logic clock can be supplied by the internal 16 MHz oscillator, an external oscillator (crystal or ceramic resonator) or a direct clock signal.

These working modes can be selected by EXT\_CLK and OSC\_SEL parameters in the CONFIG register (see [Table 23](#)).

At power-up the device starts using the internal oscillator and provides a 2 MHz clock signal on the OSCOUT pin.

---

**Attention:** In any case, before changing clock source configuration, a hardware reset is mandatory. Switching to different clock configurations during operation could cause unexpected behavior.

---

### 6.8.1 Internal oscillator

In this mode the internal oscillator is activated and OSCIN is unused. If OSCOUT clock source is enabled, the OSCOUT pin provides a 2, 4, 8 or 16 MHz clock signal (according to OSC\_SEL value); otherwise it is unused (see [Figure 7](#)).

### 6.8.2 External clock source

Two types of external clock source can be selected: crystal/ceramic resonator or direct clock source. Four programmable clock frequencies are available for each external clock source: 8, 16, 24 and 32 MHz.

When an external crystal/resonator is selected, the OSCIN and OSCOUT pins are used to drive the crystal/resonator (see [Figure 7](#)). The crystal/resonator and load capacitors (CL) must be placed as close as possible to the pins. Refer to [Table 8](#) for the choice of the load capacitor value according to the external oscillator frequency.

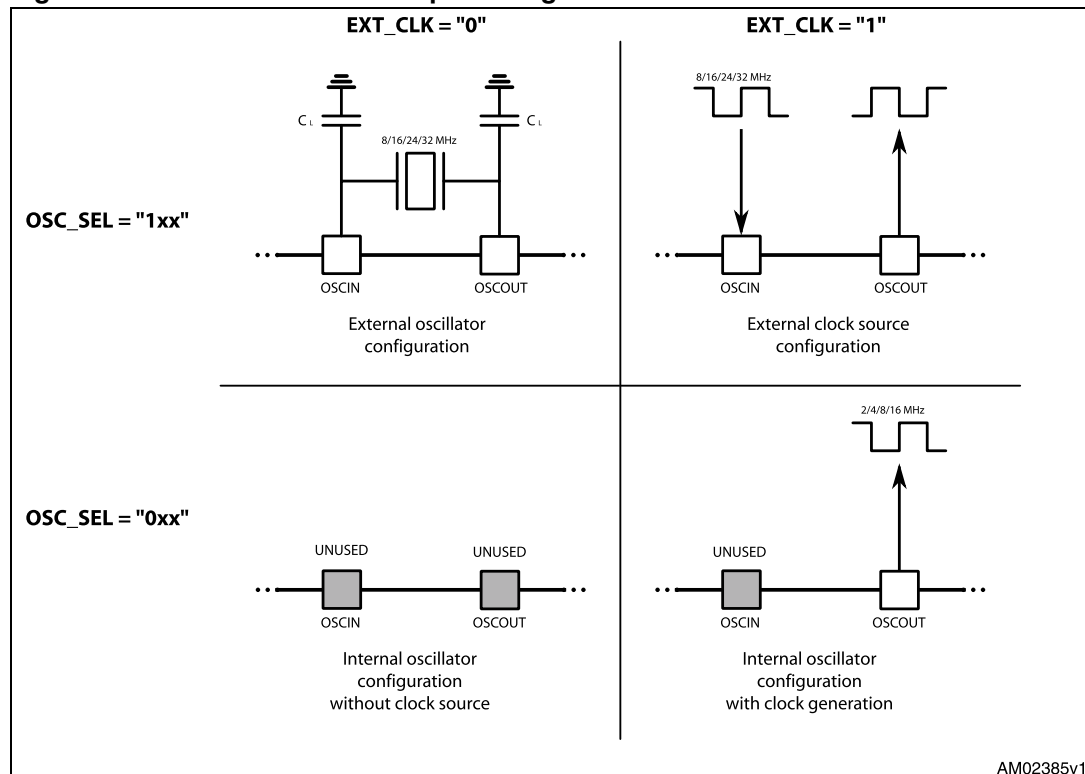
**Table 8. CL values according to external oscillator frequency**

Crystal/resonator freq. <sup>(1)</sup>	CL <sup>(2)</sup>
8 MHz	25 pF (ESR <sub>max</sub> = 80 Ω)
16 MHz	18 pF (ESR <sub>max</sub> = 50 Ω)
24 MHz	15 pF (ESR <sub>max</sub> = 40 Ω)
32 MHz	10 pF (ESR <sub>max</sub> = 40 Ω)

1. First harmonic resonance frequency.
2. Lower ESR value allows driving greater load capacitors.

If a direct clock source is used, it must be connected to the OSCIN pin and the OSCOUT pin supplies the inverted OSCIN signal (see [Figure 7](#)).

Figure 7. OSCIN and OSCOUT pin configurations



Note: When OSCIN is UNUSED, it should be left floating.  
When OSCOUT is UNUSED it should be left floating.

## 6.9 Overcurrent detection

When the current in any of the power MOSFETs exceeds a programmed overcurrent threshold, the STATUS register OCD flag is forced low until the overcurrent event has expired and a GetStatus command is sent to the IC (see [Section 9.1.13](#) and [Section 9.1.9](#)). Overcurrent event expires when all the power MOSFET currents fall below the programmed overcurrent threshold.

The overcurrent threshold can be programmed through the OCD\_TH register in one of 16 available values ranging from 375 mA to 6 A with steps of 375 mA (see [Section 9.1.9](#)).

It is possible to set whether or not an overcurrent event causes the MOSFET turn-off (bridges in high impedance status) acting on the OC\_SD bit in the CONFIG register (see [Section 9.1.12](#)). The OCD flag in the STATUS register is raised anyway (see [Table 28](#), [Section 9.1.13](#)).

When the IC outputs are turned off by an OCD event, they cannot be turned on until the OCD flag is released by a GetStatus command.

**Attention:** The overcurrent shutdown is a critical protection feature. It is not recommended to disable it.

## 6.10 Undervoltage lock-out (UVLO)

The L6474 provides a motor supply UVLO protection. When the motor supply voltage falls below the VSthOff threshold voltage, the STATUS register UVLO flag is forced low. When a GetStatus command is sent to the IC, and the undervoltage condition has expired, the UVLO flag is released (see [Section 9.1.13](#) and [Section 9.2.7](#)). Undervoltage condition expires when the motor supply voltage goes over the VSthOn threshold voltage. When the device is in undervoltage condition no motion can be performed. The UVLO flag is forced low by logic reset (power-up included) even if no UVLO condition is present.

## 6.11 Thermal warning and thermal shutdown

An internal sensor allows the L6474 to detect when the device internal temperature exceeds a thermal warning or an overtemperature threshold.

When the thermal warning threshold ( $T_{j(WRN)}$ ) is reached, the TH\_WRN bit in the STATUS register is forced low (see [Section 9.1.13](#)) until the temperature decreases below  $T_{j(WRN)}$  and a GetStatus command is sent to the IC (see [Section 9.1.13](#) and [Section 9.2.7](#)).

When the thermal shutdown threshold ( $T_{j(OFF)}$ ) is reached, the device goes into thermal shutdown condition: the TH\_SD bit in the STATUS register is forced low, the power bridges are disabled, bridges in high impedance state and the HiZ bit in the STATUS register are raised (see [Section 9.1.13](#)).

Thermal shutdown condition only expires when the temperature goes below the thermal warning threshold ( $T_{j(WRN)}$ ).

On exiting thermal shutdown condition, the bridges are still disabled (HiZ flag high).

## 6.12 Reset and standby

The device can be reset and put into standby mode through a dedicated pin. When the  $\overline{STBY\backslash RST}$  pin is driven low, the bridges are left open (High Z state), the internal charge pump is stopped, the SPI interface and control logic are disabled, and the internal 3 V voltage regulator maximum output current is reduced to  $I_{REG,STBY}$ ; as a result the L6474 heavily reduces the power consumption. At the same time the register values are reset to default and all protection functions are disabled.  $\overline{STBY\backslash RST}$  input must be forced low at least for  $t_{STBY, min.}$  in order to ensure the complete switch to standby mode.

On exiting standby mode, as well as for IC power-up, a delay of up to  $t_{logicwu}$  must be given before applying a new command to allow proper oscillator and logic startup and a delay of up to  $t_{cpwu}$  must be given to allow the charge pump startup.

On exiting standby mode the bridges are disabled (HiZ flag high).

---

**Attention:** It is not recommended to reset the device when outputs are active. The device should be switched to high impedance state before being reset.

---



## 6.13 Programmable DMOS slew-rate, dead-time and blanking-time

Using the POW\_SR parameter in the CONFIG register, it is possible to set the commutation speed of the power bridges output (see [Table 25](#)).

## 6.14 Integrated analog to digital converter

The L6474 integrates a NADC bit ramp-compare analog to digital converter with a reference voltage equal to VREG. The analog to digital converter input is available through the ADCIN pin and the conversion result is available in the ADC\_OUT register (see [Section 9.1.13](#)). Sampling frequency is equal to the clock frequency divided by 512.

The ADC\_OUT value can be used for the torque regulation or is at the user's disposal.

## 6.15 Internal voltage regulator

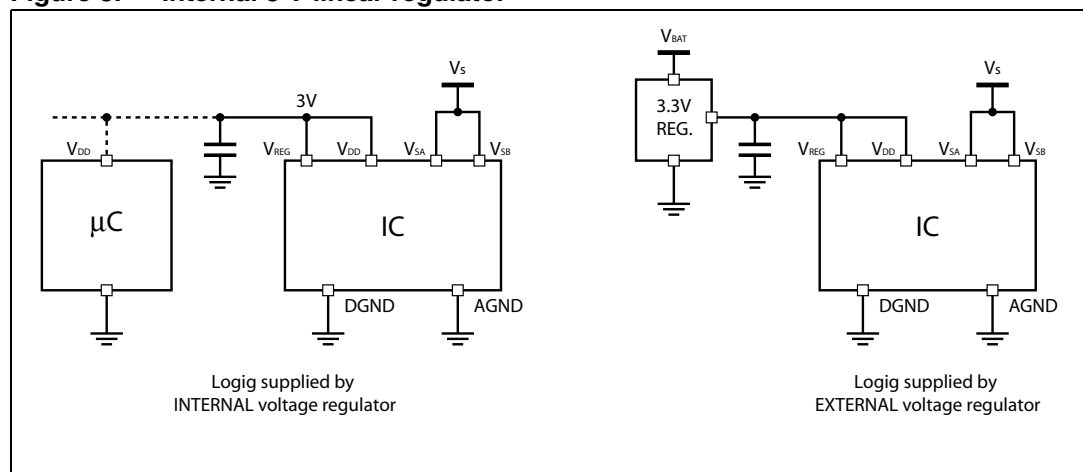
The L6474 integrates a voltage regulator which generates a 3 V voltage starting from the motor power supply (VSA and VSB). In order to make the voltage regulator stable, at least 22  $\mu\text{F}$  should be connected between the VREG pin and ground (suggested value is 47  $\mu\text{F}$ ).

The internal voltage regulator can be used to supply the VDD pin in order to make the device digital output range 3.3 V compatible ([Figure 8](#)). A digital output range 5 V compatible can be obtained connecting the VDD pin to an external 5 V voltage source. In both cases, a 10  $\mu\text{F}$  capacitance should be connected to the VDD pin in order to obtain a correct operation.

The internal voltage regulator is able to supply a current up to  $I_{\text{REG,MAX}}$ , internal logic consumption included ( $I_{\text{logic}}$ ). When the device is in standby mode the maximum current that can be supplied is  $I_{\text{REG,STBY}}$ , internal consumption included ( $I_{\text{logic,STBY}}$ ).

If an external 3.3 V regulated voltage is available, it can be applied to the VREG pin in order to supply all the internal logic and avoid power dissipation of the internal 3 V voltage regulator ([Figure 8](#)). The external voltage regulator should never sink current from the VREG pin.

**Figure 8. Internal 3 V linear regulator**



## 6.16 SYNC pin

This pin works as a synchronization signal: the output status is an echo of one of the bits of the EL\_POS register according to a SYNC\_SEL and STEP\_SEL parameter combination (see paragraph [9.1.10](#)).

## 6.17 FLAG pin

By default, an internal open drain transistor pulls the FLAG pin to ground when at least one of the following conditions occurs:

- Power-up or standby/reset exit
- Overcurrent detection
- Thermal warning
- Thermal shutdown
- UVLO
- Switch turn-on event
- Wrong command
- Non performable command.

It is possible to mask one or more alarm conditions by programming the ALARM\_EN register (see [Section 9.1.11](#), [Table 21](#)). If the corresponding bit of the ALARM\_EN register is low, the alarm condition is masked and it does not cause a FLAG pin transition; all other actions imposed by alarm conditions are performed anyway. In case of daisy-chain configuration, FLAG pins of different ICs can be or-wired to save host controller GPIOs.

## 7 Phase current control

The L6474 performs a peak current control technique described in detail in [Section 7.1](#). Furthermore, the L6474 automatically selects the best decay mode in order to follow the current profile.

Current control algorithm parameters can be programmed by T\_FAST, TON\_MIN, TOFF\_MIN and CONFIG registers (see [Section 9.1.5](#), [Section 9.1.6](#), [Section 9.1.7](#) and [Section 9.1.12](#) for details).

The current amplitude can be set through the TVAL register (see [Section 9.1.4](#)). The output current amplitude can also be regulated by ADCIN voltage value (see [Section 6.14](#)).

Each bridge is driven by an independent control system that shares with the other bridge the control parameters only.

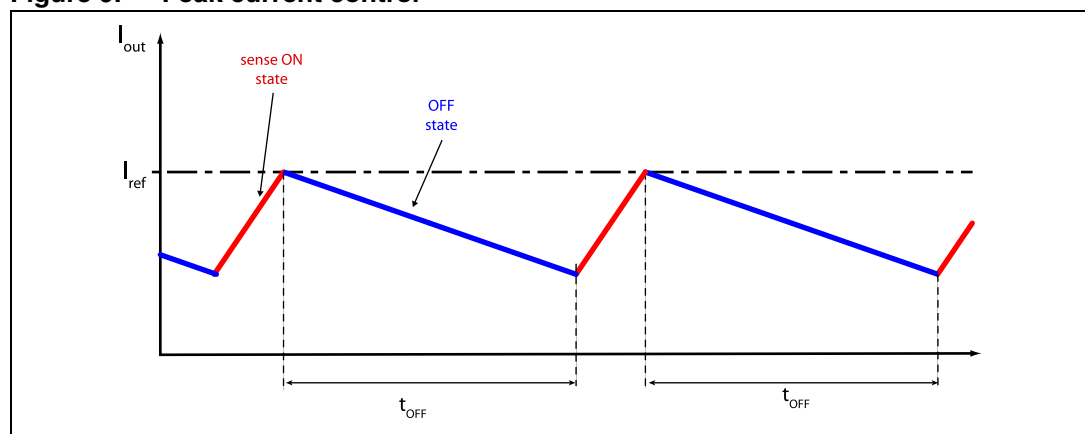
### 7.1 Peak current control

The L6474 implements a peak current control algorithm with fixed OFF time. The control cycle begins in the ON state: the opposite high-side DMOS low-side DMOS of the power bridges are turned on according to the required current direction. In this way, the phase current is increased according to the electrical model of the motor.

When the target current value is reached (this value is internally generated according to the present value of the EL\_POS register), the device switches to the OFF state in order to make the phase current decay. During the OFF state both slow and fast decay can be performed; the better decay combination is automatically selected by L6472 as described in [Section 7.2](#).

The  $t_{OFF}$  value sets through the TOFF parameter of the CONFIG register and the value of the TOFF\_MIN register. If TOFF is greater than TOFF\_MIN, it defines the OFF time of the system. Otherwise the TOFF\_MIN value is used.

**Figure 9. Peak current control**



## 7.2 Auto-adjusted decay mode

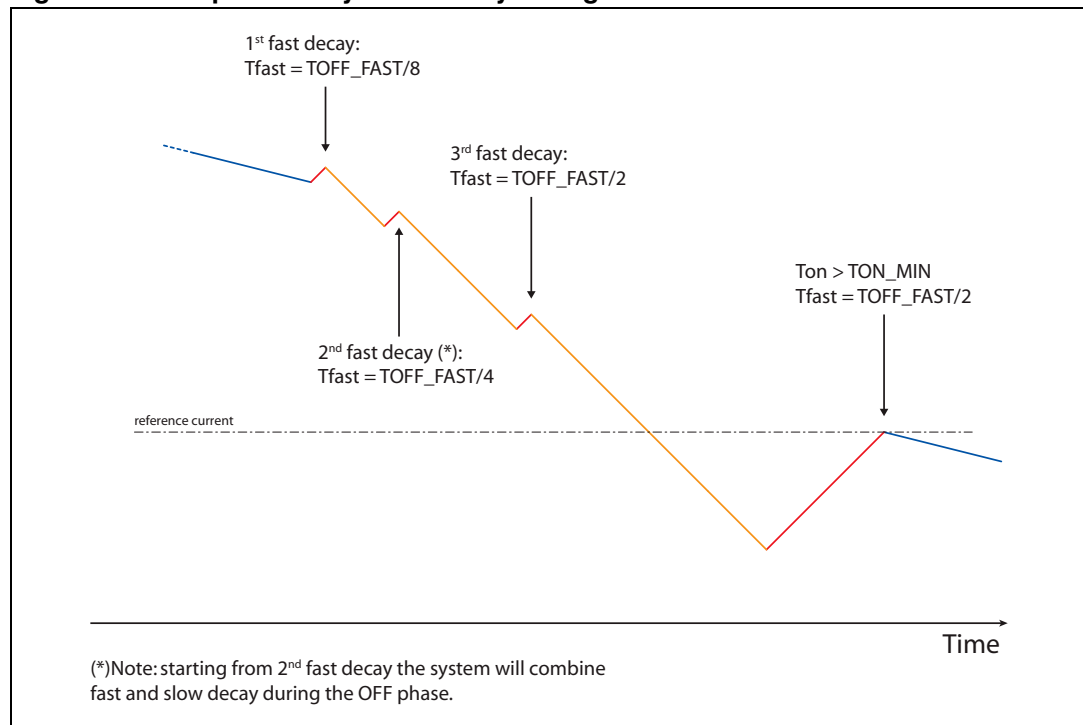
During the current control, the device automatically selects the best decay mode in order to follow the current profile reducing the current ripple.

At reset, the OFF time is performed by turning on both the low-side MOS of the power stage and the current recirculates in the lower half of the bridge (slow decay).

If, during a PWM cycle, the target current threshold is reached in a time shorter than the  $T_{ON\_MIN}$  value, a fast decay of  $TOFF\_FAST/8$  ( $T\_FAST$  register) is immediately performed, turning on the opposite MOS of both half bridges and the current recirculates back to the supply bus.

After this time, the bridge returns to the ON state: if the time needed to reach the target current value is still less than  $T_{ON\_MIN}$ , a new fast decay is performed with a period twice the previous one. Otherwise, the normal control sequence is followed as described in section 7.1. The maximum fast decay duration is set by  $TOFF\_FAST$  value.

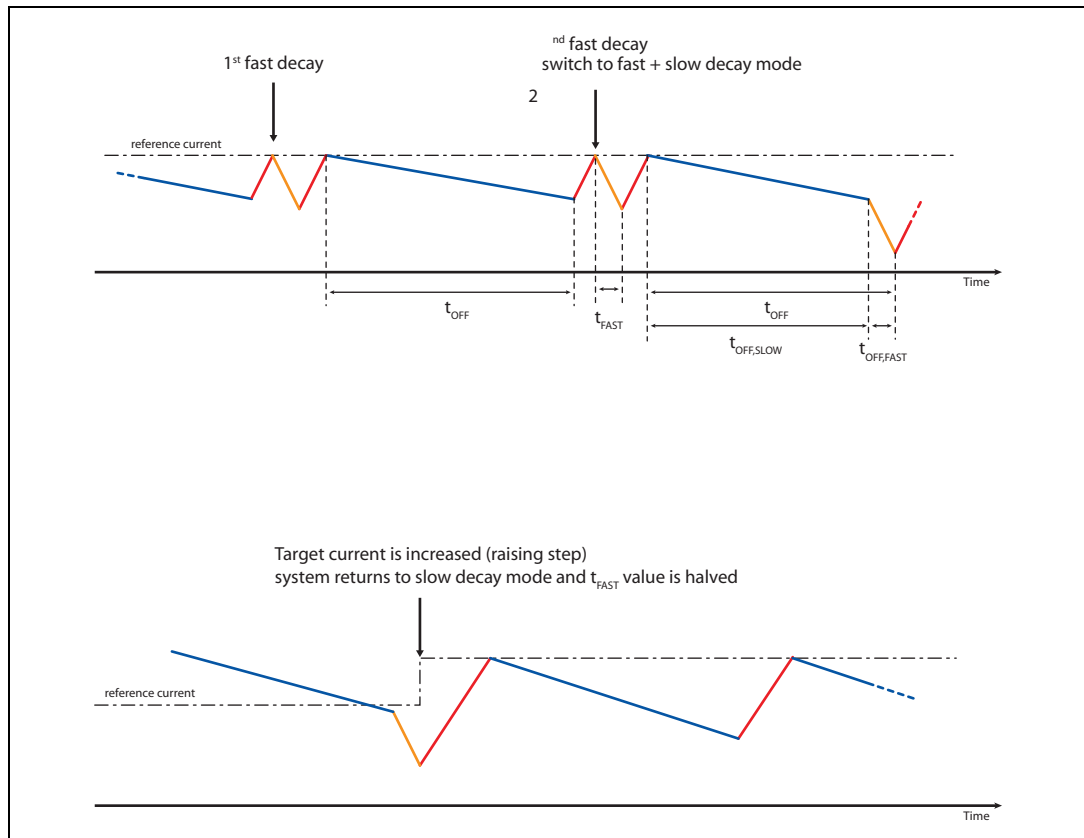
**Figure 10. Adaptive decay - fast decay tuning**



When two or more fast decays are performed with present target current, the control system adds a fast decay at the end of every OFF time, keeping the OFF state duration constant ( $t_{OFF}$  is split into  $t_{OFF,SLOW}$  and  $t_{OFF,FAST}$ ). When the current threshold is increased by a micro-step change (rising step), the system returns to normal decay mode (slow decay only) and the  $t_{FAST}$  value is halved.

Reaching the current sinewave zero crossing causes the current control system to return to the reset state.

**Figure 11. Adaptive decay - switch from normal to slow+fast decay mode and vice versa**



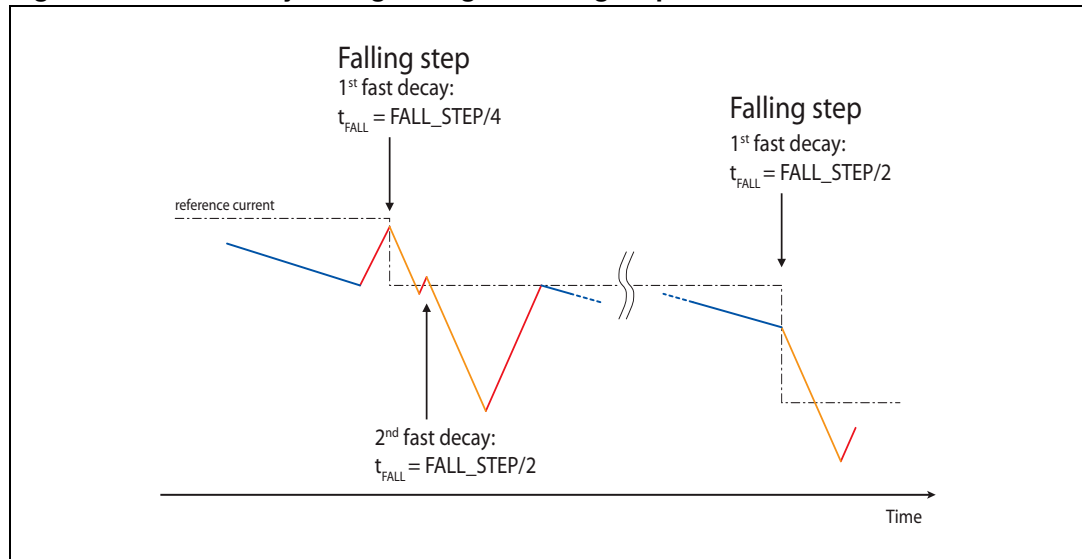
### 7.3 Auto-adjusted fast decay during the falling steps

When the target current is decreased by a micro-step change (falling step), the device performs a fast decay in order to reach the new value as fast as possible. Anyway, exceeding the fast duration could cause a strong ripple on the step change. The L6474 automatically adjusts these fast decays reducing the current ripple.

At reset, the fast decay value ( $t_{FALL}$ ) is set to  $FALL\_STEP/4$  ( $T\_FAST$  register). The  $t_{FALL}$  value is doubled every time, within the same falling step, an extra fast decay is necessary to obtain an ON time greater than  $TON\_MIN$ . The maximum  $t_{FALL}$  value is equal to  $FALL\_STEP$ .

At the next falling step, the system uses the last  $t_{FALL}$  value of the previous falling step. Stopping the motor or reaching the current sinewave zero crossing causes the current control system to return to the reset state.

Figure 12. Fast decay tuning during the falling steps



## 7.4 Torque regulation (output current amplitude regulation)

The output current amplitude can be regulated in two ways: writing the TVAL register or varying the ADCIN voltage value.

The EN\_TQREG bit (CONFIG register) sets the torque regulation method. If this bit is high, ADC\_OUT prevalue is used to regulate output current amplitude (see [Section 9.1.8](#)). Otherwise the internal analog to digital converter is at the user's disposal and the output current amplitude is managed by the TVAL register (see [Section 9.1.4](#)).

The voltage applied to the ADCIN pin is sampled at fS frequency and converted in an NADC bit digital signal. The analog to digital conversion result is available in the ADC\_OUT register.

## 8 Serial interface

The integrated 8-bit serial peripheral interface (SPI) is used for a synchronous serial communication between the host microprocessor (always master) and the L6474 (always slave).

The SPI uses chip select ( $\overline{CS}$ ), serial clock (CK), serial data input (SDI) and serial data output (SDO) pins. When  $\overline{CS}$  is high, the device is unselected and the SDO line is inactive (high-impedance).

The communication starts when  $\overline{CS}$  is forced low. The CK line is used for synchronization of data communication.

All commands and data bytes are shifted into the device through the SDI input, most significant bit first. The SDI is sampled on the rising edges of the CK.

All output data bytes are shifted out of the device through the SDO output, most significant bit first. The SDO is latched on the falling edges of the CK. When a return value from the device is not available, an all zero byte is sent.

After each byte transmission, the  $\overline{CS}$  input must be raised and be kept high for at least  $t_{disCS}$  in order to allow the device to decode the received command and put the return value into the shift register.

All timing requirements are shown in [Figure 13](#) (see respective [Section 3: Electrical characteristics](#) for values).

Multiple devices can be connected in a daisy-chain configuration, as shown in [Figure 14](#).

**Figure 13. SPI timings diagram**

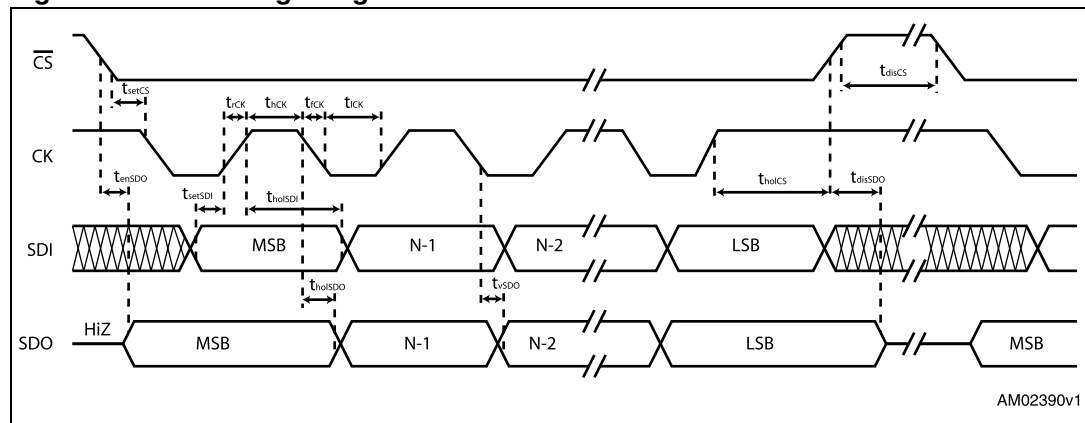
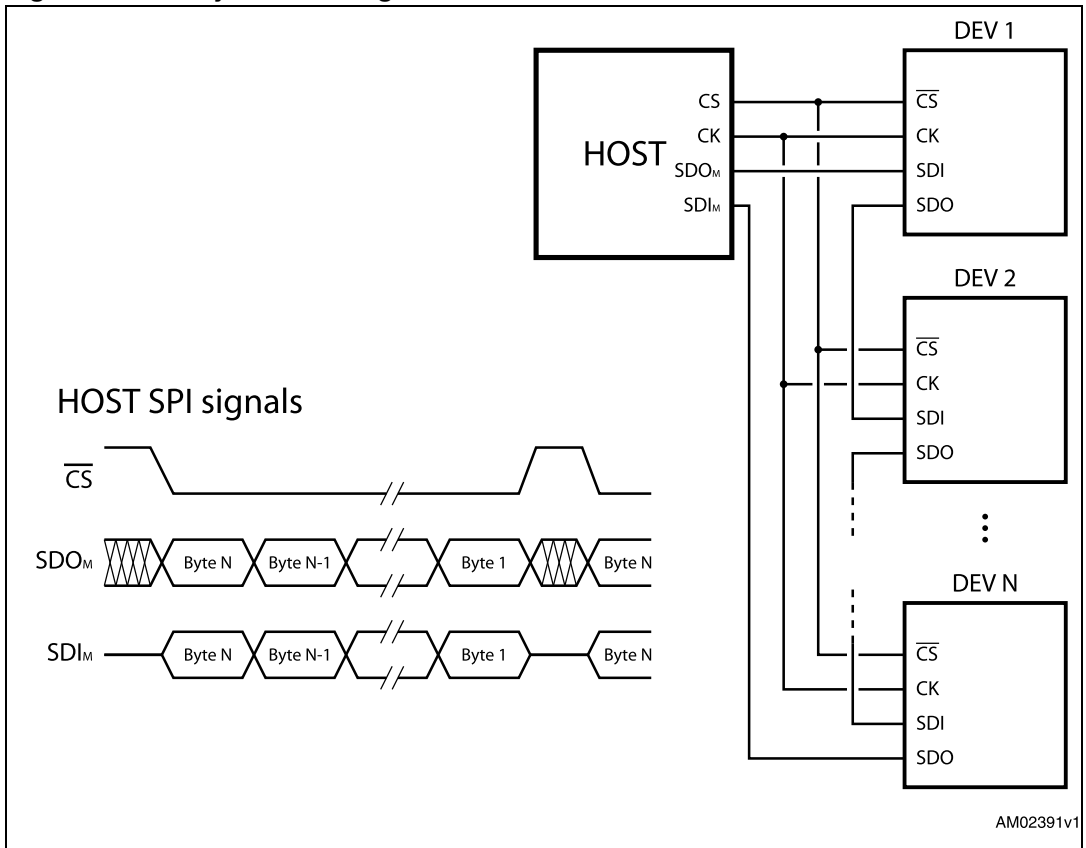


Figure 14. Daisy-chain configuration





## 9 Programming manual

### 9.1 Registers and flags description

The following is a map of the user registers available (detailed description in respective paragraphs):

**Table 9. Register map**

Address [Hex]	Register name	Register function	Len. [bit]	Reset Hex	Reset Value	Remarks (1)
h01	ABS_POS	Current position	22	000000	0	R, WR
h02	EL_POS	Electrical position	9	000	0	R, WR
h03	MARK	Mark position	22	000000	0	R, WR
h04	RESERVED	Reserved address	24			
h05	RESERVED	Reserved address	16			
h06	RESERVED	Reserved address	16			
h07	RESERVED	Reserved address	16			
h08	RESERVED	Reserved address	16			
h15	RESERVED	Reserved address	16			R, WR
h09	TVAL	Reference current	7	29	1.3125 A	R, WR
h0A	RESERVED	Reserved address	8			
h0B	RESERVED	Reserved address	8			
h0C	RESERVED	Reserved address	8			
h0D	RESERVED	Reserved address	16			
h0E	T_FAST	Fast decay/fall step time	8	19	1 $\mu$ s / 5 $\mu$ s	R, WH
h0F	TON_MIN	Minimum ON time	7	29	20.5 $\mu$ s	R, WH
h10	TOFF_MIN	Minimum OFF time	7	29	20.5 $\mu$ s	R, WH
h11	RESERVED	Reserved address	8			
h12	ADC_OUT	ADC output	5	XX <sup>(2)</sup>		R
h13	OCD_TH	OCD threshold	4	8	3.38A	R, WR
h14	RESERVED	Reserved address	8			
h16	STEP_MODE	Step mode	8	7	16 microsteps, no synch	R, WH
h17	ALARM_EN	Alarms enables	8	FF	All alarms enabled	R, WR
h18	CONFIG	IC configuration	16	2E88	Internal oscillator, 2 MHz OSCOUT clock, supply voltage compensation disabled, overcurrent shutdown enabled, slew-rate = 290 V/ $\mu$ s TOFF = 40 $\mu$ s	R, WH

**Table 9. Register map (continued)**

Address [Hex]	Register name	Register function	Len. [bit]	Reset Hex	Reset Value	Remarks (1)
h19	STATUS	Status	16	XXXX (2)	High impedance state, UVLO/Reset flag set.	R
h1A	RESERVED	Reserved address				
h1B	RESERVED	Reserved address				

1. R: Readable, WH: writable only when outputs are in high impedance, WR: always writable.
2. According to startup conditions.

### 9.1.1 ABS\_POS

The ABS\_POS register contains the current motor absolute position in agreement to the selected step mode; the stored value unit is equal to the selected step mode (full, half, quarter, etc.). The value is in 2's complement format and it ranges from  $-2^{21}$  to  $+2^{21}-1$ .

At power-on the register is initialized to "0" (HOME position).

### 9.1.2 EL\_POS

The EL\_POS register contains the current electrical position of the motor. The two MSbits indicate the current step and the other bits indicate the current microstep (expressed in step/128) within the step.

**Table 10. EL\_POS register**

Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STEP			MICROSTEP					

When the EL\_POS register is written by the user the new electrical position is instantly imposed. When the EL\_POS register is written its value must be masked in order to match with the step mode selected in the STEP\_MODE register in order to avoid a wrong microstep value generation (see [Section 9.1.10](#)); otherwise the resulting microstep sequence is incorrect.

Any attempt to write the register when the outputs are enabled causes the command to be ignored and the NOTPERF\_CMD flag to rise (see [Section 9.1.13](#)).

### 9.1.3 MARK

The MARK register contains an absolute position called MARK, according to the selected step mode; the stored value unit is equal to the selected step mode (full, half, quarter, etc.).

It is in 2's complement format and it ranges from  $-2^{21}$  to  $+2^{21}-1$ .

### 9.1.4 TVAL

The TVAL register contains the current value that is assigned to the torque regulation DAC.

The available range is from 31.25 mA to 4 A with a resolution of 31.25 mA, as shown in [Table 2](#).

**Table 11. Torque regulation register**

TVAL [6..0]							Output current amplitude
0	0	0	0	0	0	0	31.25 mA
0	0	0	0	0	0	1	62.5 mA
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	3.969 A
1	1	1	1	1	1	1	4 A

### 9.1.5 T\_FAST

The T\_FAST register contains the maximum fast decay time (TOFF\_FAST) and the maximum fall step time (FALL\_STEP) used by the current control system (see [Section 7.2](#) and [Section 7.3](#) for details):

**Table 12. T\_FAST register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOFF_FAST				FAST_STEP			

The available range for both parameters is from 2  $\mu$ s to 32  $\mu$ s.

**Table 13. Maximum fast decay times**

TOFF_FAST [3..0] FAST_STEP[3..0]				Fast decay time
0	0	0	0	2 $\mu$ s
0	0	0	1	4 $\mu$ s
⋮	⋮	⋮	⋮	⋮
1	1	1	0	28 $\mu$ s
1	1	1	1	32 $\mu$ s

Any attempt to write to the register when the outputs are enabled causes the command to be ignored and the NOTPERF\_CMD to rise (see [Section 9.1.13](#)).

### 9.1.6 TON\_MIN

The TON\_MIN register contains the minimum ON time value used by the current control system (see [Section 7.2](#)).

The available range for both parameters is from 0.5  $\mu$ s to 64  $\mu$ s.

**Table 14. Minimum ON time**

							Time
0	0	0	0	0	0	0	0.5 $\mu$ s
0	0	0	0	0	0	1	1 $\mu$ s
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	63.5 $\mu$ s
1	1	1	1	1	1	1	64 $\mu$ s

Any attempt to write to the register when the outputs are enabled causes the command to be ignored and the NOTPERF\_CMD to rise (see [Section 9.1.13](#)).

**9.1.7 TOFF\_MIN**

The TOFF\_MIN register contains the minimum OFF time value used by the current control system (see [Section 7.1](#) for details). This parameter imposes the OFF time of the current control system only if its value is greater than the TSW one.

The available range for both parameters is from 0.5  $\mu$ s to 64  $\mu$ s.

**Table 15. Minimum OFF time**

							Time
0	0	0	0	0	0	0	0.5 $\mu$ s
0	0	0	0	0	0	1	1 $\mu$ s
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	63.5 $\mu$ s
1	1	1	1	1	1	1	64 $\mu$ s

Any attempt to write to the register when the outputs are enabled causes the command to be ignored and the NOTPERF\_CMD to rise (see [Section 9.1.13](#)).

### 9.1.8 ADC\_OUT

The ADC\_OUT register contains the result of the analog to digital conversion of the ADCIN pin voltage.

Any attempt to write to the register causes the command to be ignored and the NOTPERF\_CMD flag to rise (see [Section 9.1.13](#)).

**Table 16. ADC\_OUT value and torque regulation feature**

VADCIN/ VREG	ADC_OUT [4..0]					Output current amplitude
0	0	0	0	0	0	125 mA
1/32	0	0	0	0	1	250 mA
⋮	⋮	⋮	⋮	⋮	⋮	⋮
30/32	1	1	1	1	0	3.875 A
31/32	1	1	1	1	1	4 A

### 9.1.9 OCD\_TH

The OCD\_TH register contains the overcurrent threshold value (see [Section 6.9](#) for details). The available range is from 375 mA to 6 A, steps of 375 mA as shown in [Table 17](#).

**Table 17. Overcurrent detection threshold**

OCD_TH [3..0]				Overcurrent detection threshold
0	0	0	0	375 mA
0	0	0	1	750 mA
⋮	⋮	⋮	⋮	⋮
1	1	1	0	5.625 A
1	1	1	1	6 A

### 9.1.10 STEP\_MODE

The STEP\_MODE register has the following structure:

**Table 18. STEP\_MODE register**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	SYNC_SEL			1 <sup>(1)</sup>	STEP_SEL		

1. When the register is written this bit should be set to 1.

The STEP\_SEL parameter selects one of five possible stepping modes:

**Table 19. Step mode selection**

STEP_SEL[2..0]			Step mode
0	0	0	Full step
0	0	1	Half step
0	1	0	1/4 microstep
0	1	1	1/8 microstep
1	X	X	1/16 microstep

Every time the step mode is changed, the electrical position (i.e. the point of microstepping sinewave that is generated) is reset to the first microstep.

---

**Warning: Every time STEP\_SEL is changed the value in ABS\_POS register loses meaning and should be reset.**

---

Any attempt to write the register when the outputs are enabled causes the command to be ignored and the NOTPERF\_CMD flag to rise (see [Section 9.1.13](#)).

The SYNC output provides a synchronization signal according to SYNC\_SEL parameter.

The synchronization signal is obtained starting from electrical position information (EL\_POS register) according to [Table 10](#):

**Table 20. SYNC signal source**

SYNC_SEL[2..0]			Source
0	0	0	EL_POS[7]
0	0	1	EL_POS[6]
0	1	0	EL_POS[5]
0	1	1	EL_POS[4]
1	0	0	EL_POS[3]
1	0	1	UNUSED <sup>(1)</sup>
1	1	0	UNUSED <sup>(1)</sup>
1	1	1	UNUSED <sup>(1)</sup>

1. When this value is selected the BUSY output is forced low.

### 9.1.11 ALARM\_EN

The ALARM\_EN register allows to select which alarm signals are used to generate the FLAG output. If the respective bit of the ALARM\_EN register is set high, the alarm condition forces the FLAG pin output down.

**Table 21. ALARM\_EN register**

ALARM_EN bit	Alarm condition
0 (LSB)	Overcurrent
1	Thermal shutdown
2	Thermal warning
3	Undervoltage
4	RESERVED
5	RESERVED
6	Switch turn-on event
7 (MSB)	Wrong or not performable command

### 9.1.12 CONFIG

The CONFIG register has the following structure:

**Table 22. CONFIG register**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0	TOFF					POW_SR	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OC_SD	RESERVED	EN_TQREG	0	EXT_CLK	OSC_SEL		



The OSC\_SEL and EXT\_CLK bits set the system clock source:

**Table 23. Oscillator management**

EXT_CLK	OSC_SEL[2..0]			Clock source	OSCIN	OSCOUT
0	0	0	0	Internal oscillator: 16 MHz	Unused	Unused
0	0	0	1			
0	0	1	0			
0	0	1	1			
1	0	0	0	Internal oscillator: 16 MHz	Unused	Supplies a 2 MHz clock
1	0	0	1	Internal oscillator: 16 MHz	Unused	Supplies a 4 MHz clock
1	0	1	0	Internal oscillator: 16 MHz	Unused	Supplies a 8 MHz clock
1	0	1	1	Internal oscillator: 16 MHz	Unused	Supplies a 16 MHz clock
0	1	0	0	External crystal or resonator: 8 MHz	Crystal/resonator driving	Crystal/resonator driving
0	1	0	1	External crystal or resonator: 16 MHz	Crystal/resonator driving	Crystal/resonator driving
0	1	1	0	External crystal or resonator: 24 MHz	Crystal/resonator driving	Crystal/resonator driving
0	1	1	1	External crystal or resonator: 32 MHz	Crystal/resonator driving	Crystal/resonator driving
1	1	0	0	Ext. clock source: 8 MHz (Crystal/resonator driver disabled)	Clock source	Supplies inverted OSCIN signal
1	1	0	1	Ext. clock source: 16 MHz (Crystal/resonator driver disabled)	Clock source	Supplies inverted OSCIN signal
1	1	1	0	Ext. clock source: 24 MHz (Crystal/resonator driver disabled)	Clock source	Supplies inverted OSCIN signal
1	1	1	1	Ext. clock source: 32 MHz (Crystal/resonator driver disabled)	Clock source	Supplies inverted OSCIN signal

The OC\_SD bit sets whether or not an overcurrent event causes the bridges to turn off; the OCD flag in the status register is forced low anyway:

**Table 24. Overcurrent event**

OC_SD	Overcurrent event
1	Bridges shut down
0	Bridges do not shut down

The POW\_SR bits set the slew rate value of power bridge output:

**Table 25. Programmable power bridge output slew-rate values**

POW_SR [1..0]		Output Slew-rate (1) [V/μs] <sup>(1)</sup>
0	0	320
0	1	75
1	0	110
1	1	260

1. See SRout\_r and SRout\_f parameters in the electrical characteristics [Table 5](#) for details.

The TQREG bit sets if the torque regulation (see [Section 7.4](#)) is performed through the ADCIN voltage (external) or TVAL register (internal):

**Table 26. External torque regulation enable**

TQREG	External torque regulation enable
0	Internal registers
1	ADC input

The TOFF time is used by current control system. If its value is lower than the TOFF\_MIN one, the OFF time is equal to TOFF\_MIN.

**Table 27. OFF time**

TOFF [4..0]					OFF time
0	0	0	0	0	4 μs
0	0	0	0	1	4 μs
0	0	0	1	0	8 μs
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	124 μs

Any attempt to write the CONFIG register when the outputs are enabled causes the command to be ignored and the NOTPERF\_CMD flag to rise (see [Section 9.1.13](#)).

### 9.1.13 STATUS

**Table 28. STATUS register**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	1	1	OCD	TH_SD	TH_WRN	UVLO	WRONG_CMD
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NOTPERF_CMD	0	0	DIR	0	0	1	HiZ

When HiZ flag is high, it indicates that the bridges are in high impedance state. Enable command makes the device exit from High Z state unless error flags forcing a High Z state are active.



The UVLO flag is active low and is set by an undervoltage lock-out or reset events (power-up included). The TH\_WRN, TH\_SD, OCD flags are active low and indicate, respectively, thermal warning, thermal shutdown and overcurrent detection events.

The NOTPERF\_CMD and WRONG\_CMD flags are active high and indicate, respectively, that the command received by SPI can't be performed or does not exist at all.

The UVLO, TH\_WRN, TH\_SD, OCD, NOTPERF\_CMD and WRONG\_CMD flags are latched: when the respective conditions make them active (low or high), they remain in that state until a GetStatus command is sent to the IC.

The DIR bit indicates the current motor direction:

**Table 29. STATUS register DIR bit**

DIR	Motor direction
1	Forward
0	Reverse

Any attempt to write to the register causes the command to be ignored and the NOTPERF\_CMD to rise (see [Section 9.1.13](#)).

## 9.2 Application commands

The commands summary is given in [Table 30](#).

**Table 30. Application commands**

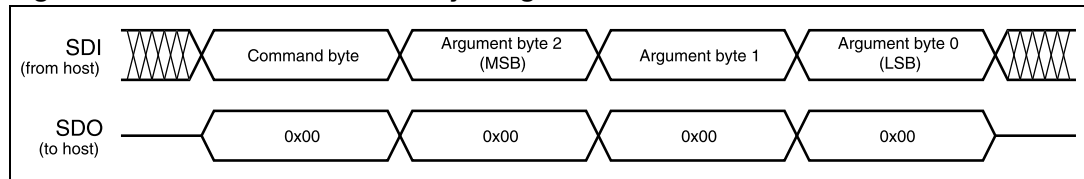
Command Mnemonic	Command binary code					Action
	[7..5]	[4]	[3]	[2..1]	[0]	
NOP	000	0	0	00	0	Nothing
SetParam(PARAM,VALUE)	000	[PARAM]				Writes VALUE in PARAM register
Enable	101	1	1	00	0	Enable the power stage
Disable	101	0	1	00	0	Puts the bridges in High Impedance status immediately
GetStatus	110	1	0	00	0	Returns the status register value
RESERVED	111	0	1	01	1	RESERVED COMMAND
RESERVED	111	1	1	00	0	RESERVED COMMAND

### 9.2.1 Command management

The host microcontroller can control motor motion and configure the L6474 through a complete set of commands.

All commands are composed of a single byte. After the command byte, some bytes of arguments should be needed (see [Figure 15](#)). Argument length can vary from 1 to 3 bytes.

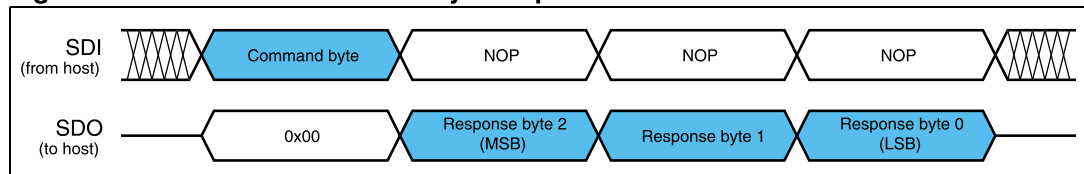
**Figure 15. Command with three-byte argument**



By default, the device returns an all zeroes response for any received byte, the only exceptions are GetParam and GetStatus commands. When one of these commands is received, the following response bytes represent the related register value (see [Figure 16](#)).

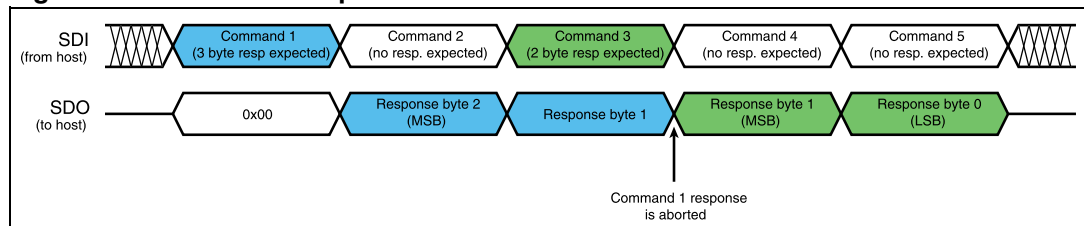
Response length can vary from 1 to 3 bytes.

**Figure 16. Command with three-byte response**



During response transmission, new commands can be sent. If a command requiring a response is sent before the previous response is completed, the response transmission is aborted and the new response is loaded into the output communication buffer (see [Figure 17](#)).

**Figure 17. Command response aborted**



When a byte that does not correspond to a command is sent to the IC it is ignored and the WRONG\_CMD flag in the STATUS register is raised (see [Section 9.1.13](#)).

### 9.2.2 Nop

**Table 31. Nop command structure**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	0	0	0	From host

Nothing is performed.

### 9.2.3 SetParam (PARAM, VALUE)

**Table 32. SetParam command structure**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	PARAM					From host
VALUE Byte 2 (if needed)								
VALUE Byte 1 (if needed)								
VALUE Byte 0								

The SetParam command sets the PARAM register value equal to VALUE; PARAM is the respective register address listed in [Table 16](#).

The command should be followed by the new register VALUE (most significant byte first). The number of bytes composing the VALUE argument depends on the length of the target register (see [Table 16](#)).

Some registers cannot be written (see [Table 16](#)); any attempt to write one of those registers causes the command to be ignored and the WRONG\_CMD flag to rise at the end of command byte, the same is true when an unknown command code is sent (see [Section 9.1.13](#)).

Some registers can only be written in particular conditions (see [Table 16](#)); any attempt to write one of those registers when the conditions are not satisfied causes the command to be ignored and the NOTPERF\_CMD flag to rise at the end of last argument byte (see [Section 9.1.13](#)).

Any attempt to set an inexistent register (wrong address value) causes the command to be ignored and the WRONG\_CMD flag to rise at the end of command byte, the same is true when an unknown command code is sent.

### 9.2.4 GetParam (PARAM)

**Table 33. GetParam command structure**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	1	PARAM					from host
ANS Byte 2 (if needed)								to host
ANS Byte 1 (if needed)								to host
ANS Byte 0								to host

This command reads the current PARAM register value; PARAM is the respective register address listed in [Table 16](#).

The command response is the current value of the register (most significant byte first). The number of bytes composing the command response depends on the length of the target register (see [Table 16](#)).

The returned value is the register one at the moment of GetParam command decoding. If register values change after this moment the response is not accordingly updated.

All registers can be read anytime.

Any attempt to read an inexistent register (wrong address value) causes the command to be ignored and the `WRONG_CMD` flag to rise at the end of command byte, the same is true when an unknown command code is sent.

### 9.2.5 Enable

**Table 34. HardStop command structure**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	0	1	1	1	0	0	0	from host

The Enable command turns on the power stage of the device.

When the motor is in high-impedance state, an Enable command forces the bridges to exit from high impedance state.

This command can be given anytime and is immediately executed.

### 9.2.6 Disable

**Table 35. Disable command structure**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	0	1	0	1	0	0	0	from host

The Disable command immediately disables the power bridges (high-impedance state) and raises the HiZ flag.

This command can be given anytime and is immediately executed.

### 9.2.7 GetStatus

**Table 36. GetStatus command structure**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	1	0	1	0	0	0	0	from host
STATUS MSByte								to host
STATUS LSByte								to host

The GetStatus command returns the Status register value. The GetStatus command resets the STATUS register warning flags. The command forces the system to exit from any error state. The GetStatus command DOES NOT reset the HiZ flag.

## 10 Package mechanical data

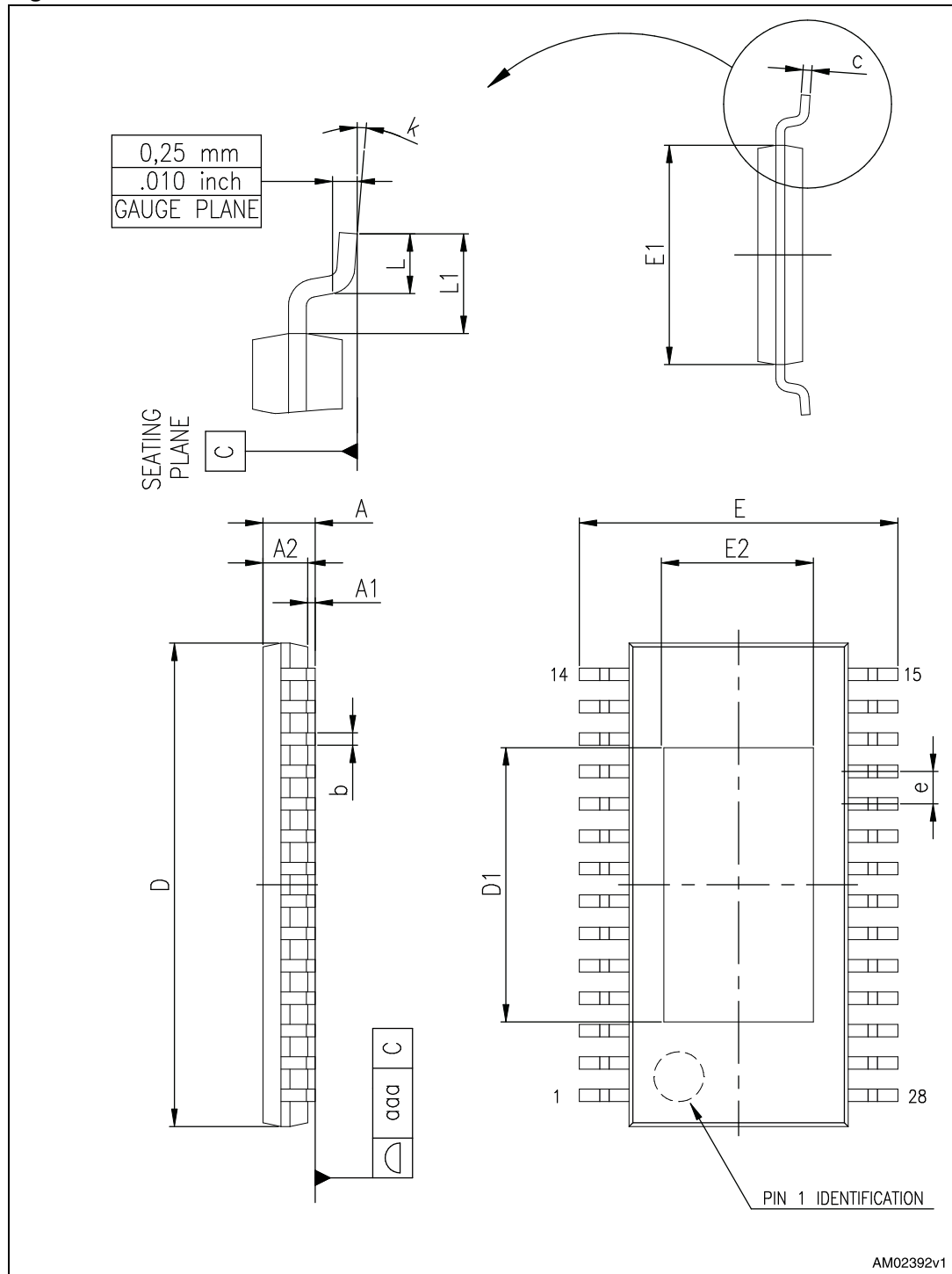
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**Table 37. HTSSOP28 mechanical data**

Dim	mm		
	Min.	Typ.	Max.
A			1.2
A1			0.15
A2	0.8	1.0	1.05
b	0.19		0.3
c	0.09		0.2
D <sup>(1)</sup>	9.6	9.7	9.8
D1		5.5	
E	6.2	6.4	6.6
E1 <sup>(2)</sup>	4.3	4.4	4.5
E2		2.8	
e		0.65	
L	0.45	0.6	0.75
L1		1.0	
K	0°		8°
aaa		0.1	

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs do not exceed 0.15 mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions do not exceed 0.25 mm per side.

Figure 18. HTSSOP28 mechanical data



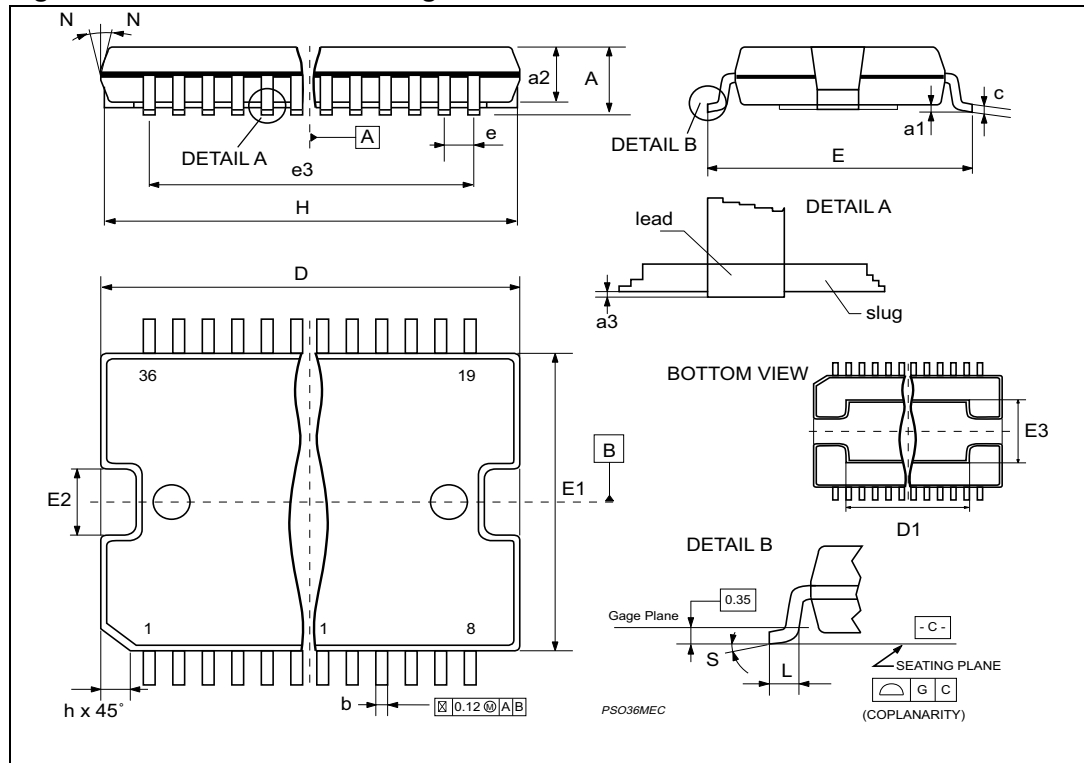
AM02392v1



Table 38. POWERSO36 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.60			0.1417
a1	0.10		0.30	0.003		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.22		0.38	0.008		0.0150
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.622		0.6299
D1	9.40		9.80	0.370		0.3858
E	13.90		14.50	0.547		0.5709
E1 (1)	10.90		11.10	0.429		0.4370
E2			2.90			0.1142
E3	5.8		6.2	0.228		0.2441
e		0.65			0.025	
e3		11.05			0.435	
G	0		0.10	0.000		0.0039
H	15.50		15.90	0.610		0.6260
h			1.10			0.0433
L	0.80		1.10	0.031		0.0433
N			10°			10°
S	0°		8°	0°		8°

Figure 19. POWERSO36 drawings



# 11 Revision history

**Table 39. Document revision history**

Date	Revision	Changes
02-Dec-2011	1	Initial release.
22-Dec-2011	2	Deleted previous chapter 6.4.1 Automatic full-step mode. Minor text changes.
20-Dec-2012	3	Changed $T_{OP}$ value and $P_{tot}$ value in <a href="#">Table 2</a> . Removed $T_j$ parameter in <a href="#">Table 3</a> . Added typical values to <a href="#">Table 4</a> . Updated HTSSOP28 mechanical data. Minor text changes.

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