International
IOR Rectifier

Data Sheet No. PD60240 revA

IRS20124S(PbF)

DIGITAL AUDIO DRIVER WITH DISCRETE DEAD-TIME AND PROTECTION

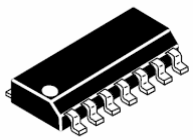
Features

- 200V high voltage ratings deliver up to 1000W output power in Class D audio amplifier applications
- Integrated dead-time generation and bi-directional over current sensing simplify design
- Programmable compensated preset dead-time for improved THD performances over temperature
- High noise immunity
- Shutdown function protects devices from overload conditions
- Operates up to 1MHz
- 3.3V/5V logic compatible input

Product Summary

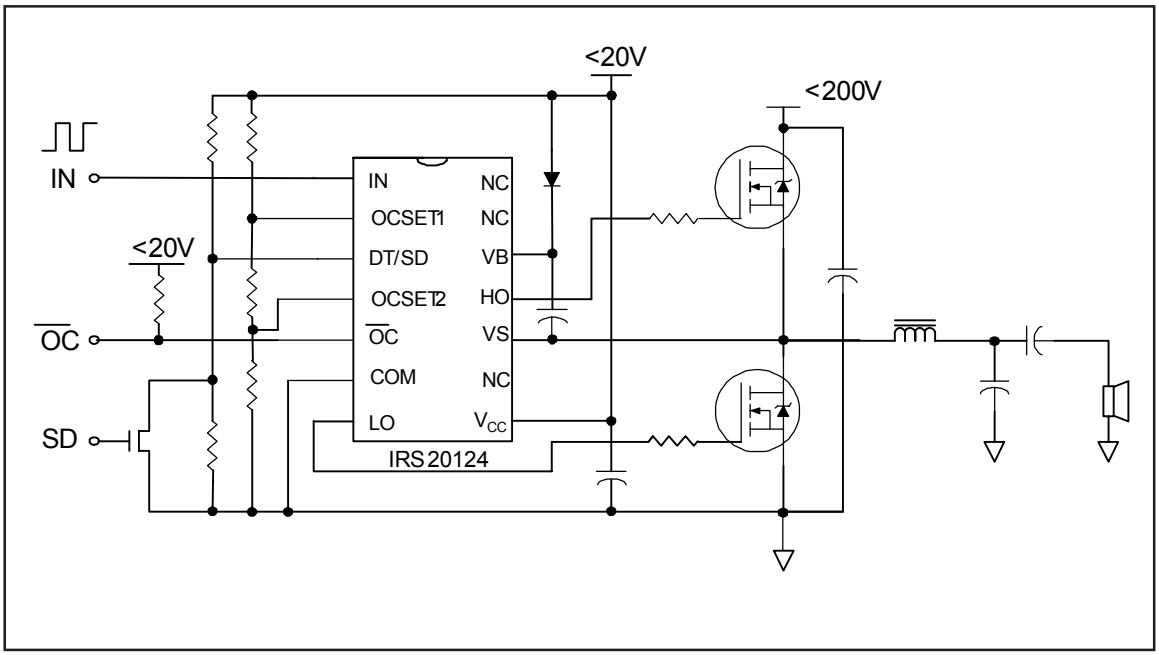
V_{SUPPLY}	200V max.
I_O+/-	1A / 1.2A typ.
Selectable Dead Time	15/25/35/45ns typ.
Prop Delay Time	70ns typ.
Bi-directional Over Current Sensing	

Package



14-Lead SOIC

Typical Application Diagram



Description

The IRS20124S is a high voltage, high speed power MOSFET driver with internal dead-time and shutdown functions specially designed for Class D audio amplifier applications.

The internal dead time generation block provides accurate gate switch timing and enables tight dead-time settings for better THD performances.

In order to maximize other audio performance characteristics, all switching times are designed for immunity from external disturbances such as VCC perturbation and incoming switching noise on the DT pin. Logic inputs are compatible with LSTTL output or standard CMOS down to 3.0V without speed degradation. The output drivers feature high current buffers capable of sourcing 1.0A and sinking 1.2A. Internal delays are optimized to achieve minimal dead-time variations. Proprietary HVIC and latch immune CMOS technologies guarantee operation down to Vs= –4V, providing outstanding capabilities of latch and surge immunities with rugged monolithic construction.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. All currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	220	V
V_S	High side floating supply voltage	VB-20	VB+0.3	V
V_{HO}	High side floating output voltage	Vs-0.3	VB+0.3	V
V_{CC}	Low side fixed supply voltage	-0.3	20	V
V_{LO}	Low side output voltage	-0.3	Vcc+0.3	V
V_{IN}	Input voltage	-0.3	Vcc+0.3	V
V_{OC}	OC pin input voltage	-0.3	Vcc+0.3	V
V_{OCSET1}	OCSET1 pin input voltage	-0.3	Vcc+0.3	V
V_{OCSET2}	OCSET2 pin input voltage	-0.3	Vcc+0.3	V
dVs/dt	Allowable Vs voltage slew rate	-	50	V/ns
Pd	Maximum power dissipation	-	1.25	W
Rth_{JA}	Thermal resistance, Junction to ambient	-	100	°C/W
T_J	Junction Temperature	-	150	°C
T_S	Storage Temperature	-55	150	°C
T_L	Lead temperature (Soldering, 10 seconds)	-	300	°C

Recommended Operating Conditions

For Proper operation, the device should be used within the recommended conditions. The Vs and COM offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	Vs+10	Vs+18	V
V_S	High side floating supply offset voltage	Note 1	200	V
V_{HO}	High side floating output voltage	Vs	V_B	V
V_{CC}	Low side fixed supply voltage	10	18	V
V_{LO}	Low side output voltage	0	VCC	V
V_{IN}	Logic input voltage	0	VCC	V
V_{OC}	OC pin input voltage	0	VCC	V
V_{OCSET1}	OCSET1 pin input voltage	0	VCC	V
V_{OCSET2}	OCSET2 pin input voltage	0	VCC	V
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S equal to -8V to 200V. Logic state held for V_S equal to -8V to -V_{BS}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1nF and T_A = 25°C unless otherwise specified. Figure 2 shows the timing definitions.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	High & low side turn-on propagation delay	—	60	80	nsec	V_S=0V
t_{off}	High & low side turn-off propagation delay	—	60	80		V_S=200V
t_r	Turn-on rise time	—	25	40		
t_f	Turn-off fall time	—	15	35		
tsd	Shutdown propagation delay	—	140	200		
toc	Propagation delay time from Vs>Vsoc+ to OC	—	280	—		OC_{SET1}=3.22V OC_{SET2}=1.20V
twoc min	OC pulse width	—	100	—		
toc filt	OC input filter time	—	200	—		
DT1	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	0	15	40		V_{DT}>V_{DT1}
DT2	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	5	25	50		V_{DT1}>V_{DT}> V_{DT2}
DT3	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	10	35	60		V_{DT2}>V_{DT}> V_{DT3}
DT4	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})V_DT= V_{DT4}	15	45	70		V_{DT3}>V_{DT}> V_{DT4}

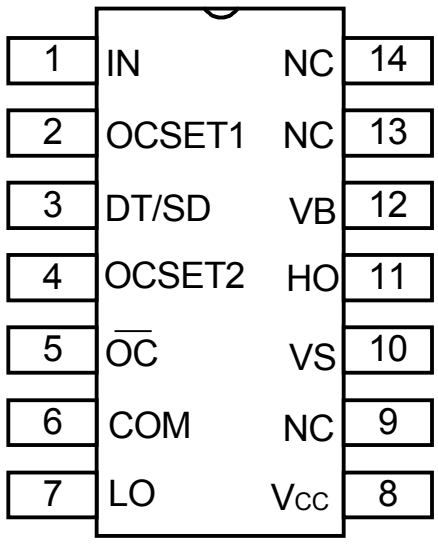
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic high input voltage	2.5	—	—	V	Vcc=10~20V
V_{IL}	Logic low input voltage	—	—	1.2		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	1.2		Io=0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		Io=0A
UV_{CC+}	Vcc supply UVLO positive threshold	8.3	9.0	9.7		
UV_{CC-}	Vcc supply UVLO negative threshold	7.5	8.2	8.9		
UV_{BS+}	High side well UVLO positive threshold	8.3	9.0	9.7		
UV_{BS-}	High side well UVLO negative threshold	7.5	8.2	8.9		
I_{QBS}	High side quiescent current	—	—	1	mA	
I_{QCC}	Low side quiescent current	—	—	4		$V_{DT} = V_{CC}$
I_{LK}	High to Low side leakage current	—	—	50	µA	$V_B = V_S$ =200V
I_{IN+}	Logic “1” input bias current	—	3	10		V_{IN} =3.3V
I_{IN-}	Logic “0” input bias current	—	0	1.0		V_{IN} =0V
I_{o+}	Output high short circuit current (Source)	—	1.0	—	A	Vo=0V, PW<10µS
I_{o-}	Output low short circuit current (Sink)	—	1.2	—		Vo=15V, PW<10µS
V_{DT1}	DT mode select threshold 1	0.8xVcc	0.89xVcc	0.97xVcc	V	
V_{DT2}	DT mode select threshold 2	0.51xVcc	0.57xVcc	0.63xVcc		
V_{DT3}	DT mode select threshold 3	0.32xVcc	0.36xVcc	0.40xVcc		
V_{DT4}	DT mode select threshold 4	0.21xVcc	0.23xVcc	0.25xVcc		
V_{SOC+}	Positive OC threshold in Vs	0.75	1.0	1.25		OC_{SET1}=3.22V OC_{SET}2=1.20
V_{SOC-}	Negative OC threshold in Vs	-1.25	-1.0	-0.75		OC_{SET1}=3.22V OC_{SET2}=1.20V

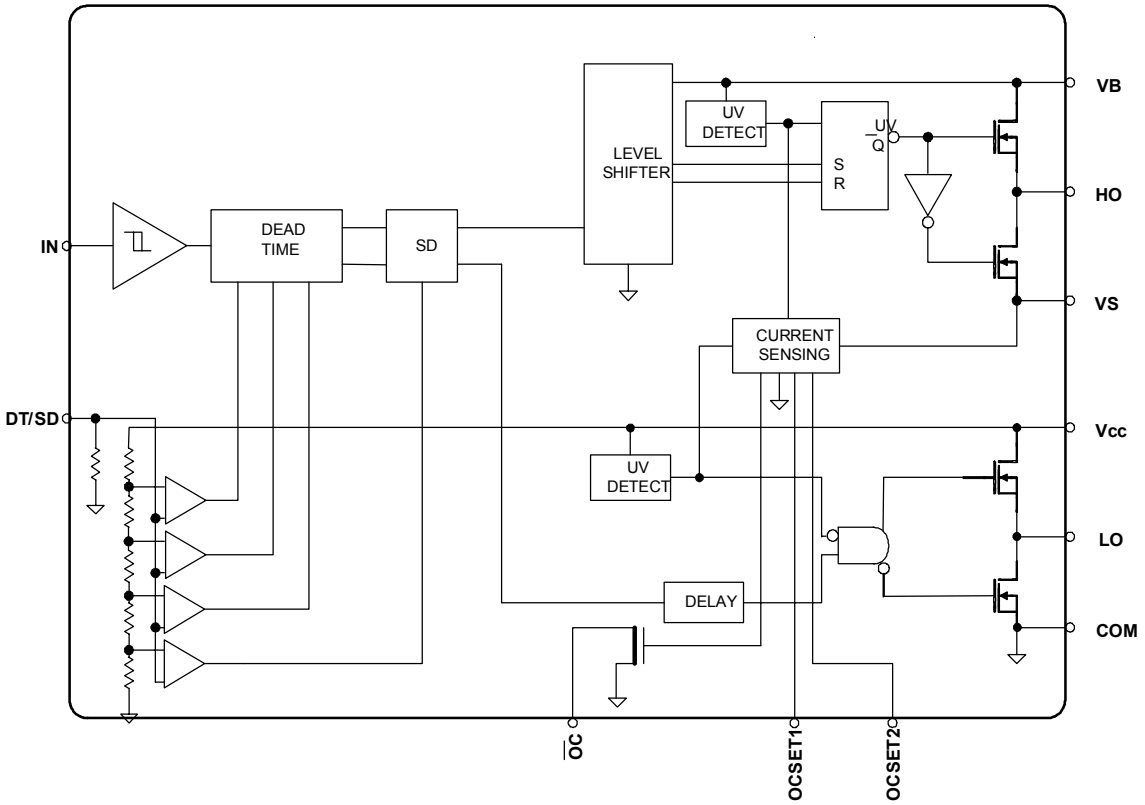
Lead Definitions

Symbol	Description
VCC	Low side logic Supply voltage
VB	High side floating supply
HO	High side output
VS	High side floating supply return
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
DT/SD	Input for programmable dead-time, referenced to COM. Shutdown LO and HO when tied to COM
COM	Low side supply return
LO	Low side output
OC	Over current output (negative logic)
OC_{SET1}	Input for setting negative over current threshold
OC_{SET2}	Input for setting positive over current threshold



IR20124S 14 Lead SOIC (narrow body)

Block Diagram



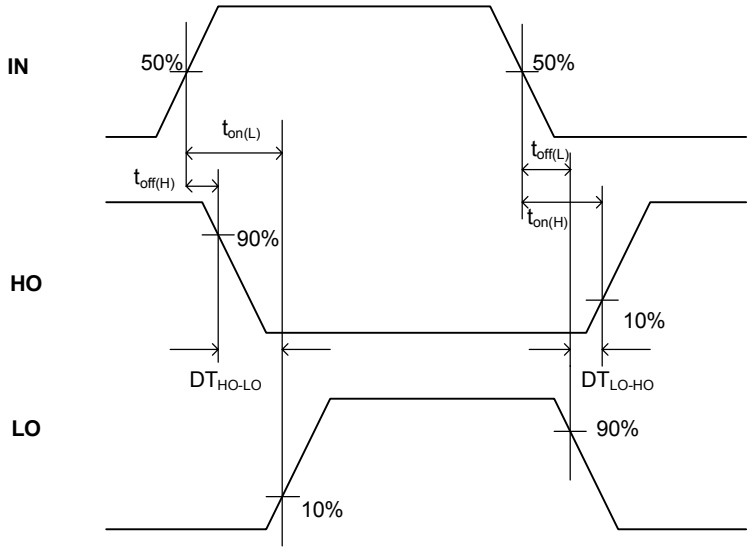


Figure 1. Switching Time Waveform Definitions

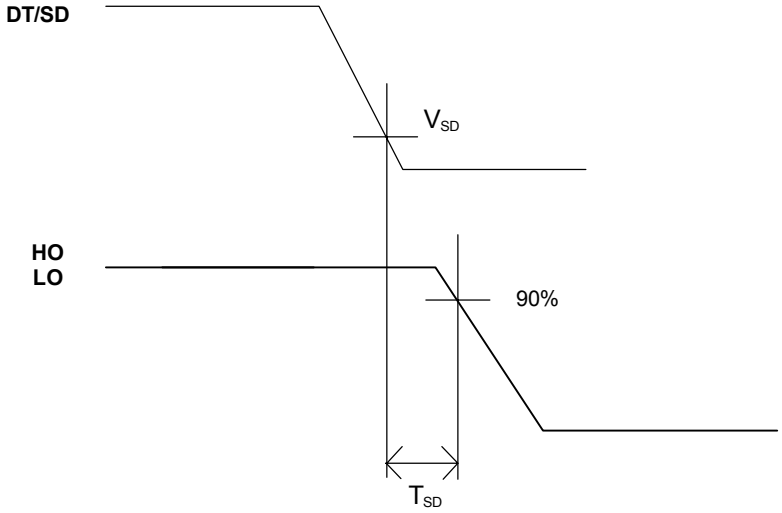


Figure 2. Shutdown Waveform Definitions

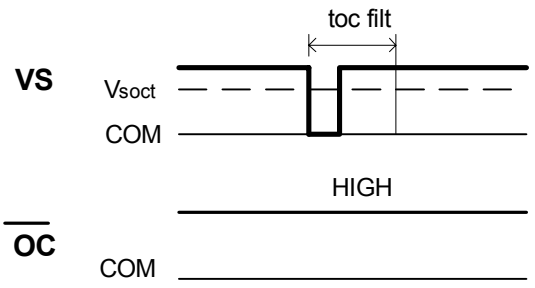


Figure 3. OC Input FilterTime Definitions

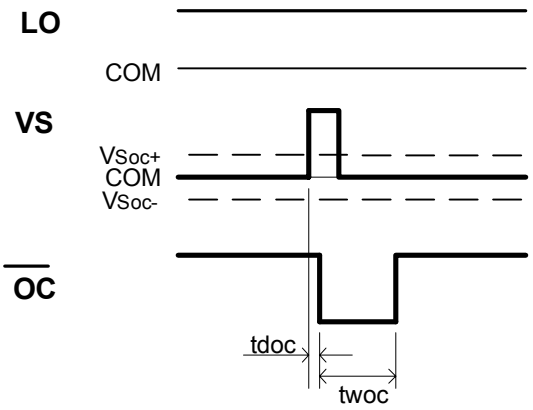


Figure 4. OC Waveform Definitions

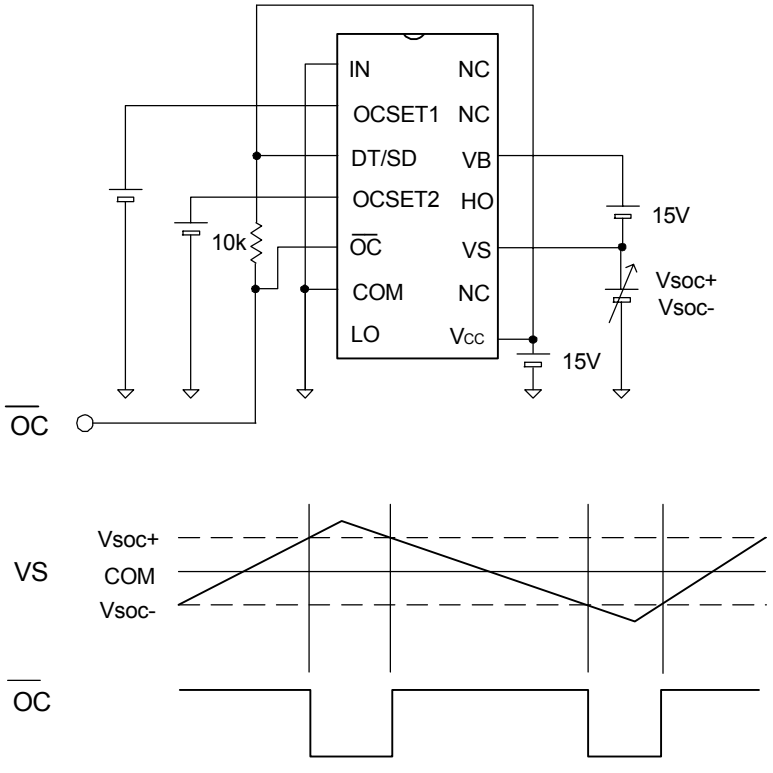


Figure 5. OC Waveform Definitions

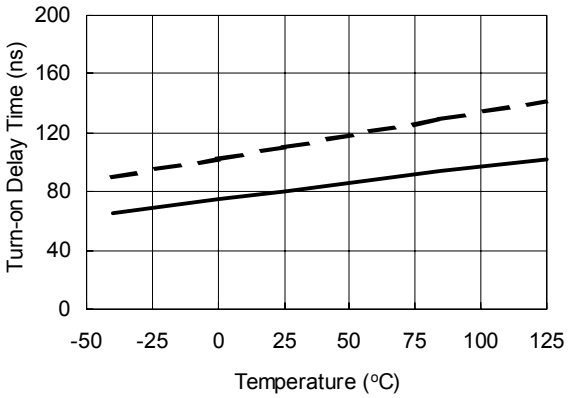


Figure 6A. Turn-On Time vs. Temperature

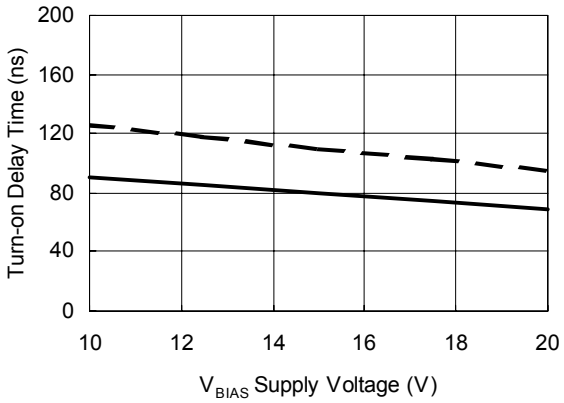


Figure 6B. Turn-On Time vs. Supply Voltage

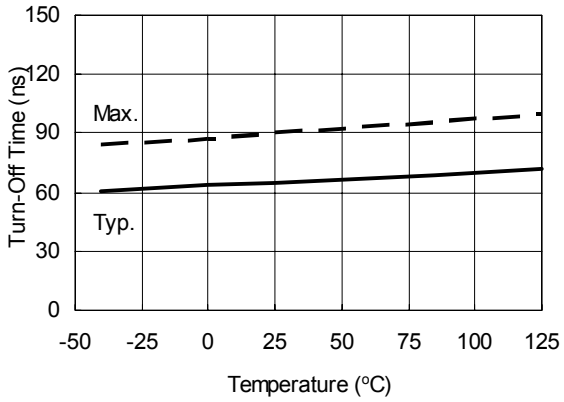


Figure 7A. Turn-Off Time vs. Temperature

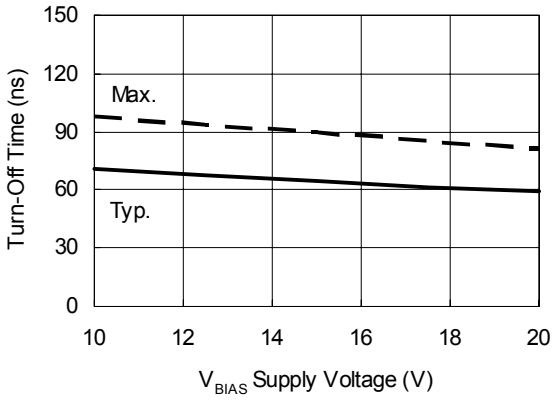
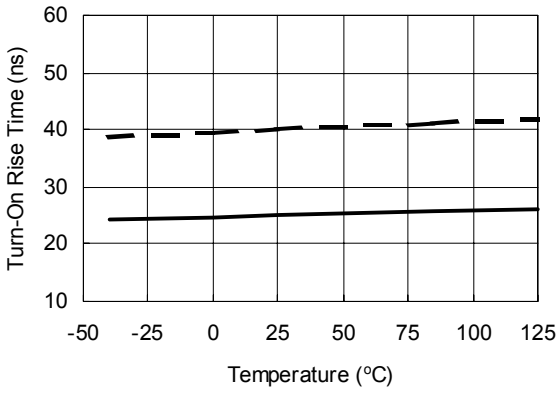


Figure 7B. Turn-Off Time vs. Supply Voltage



Fiure 8A. Turn-On Rise Time vs.Temperature

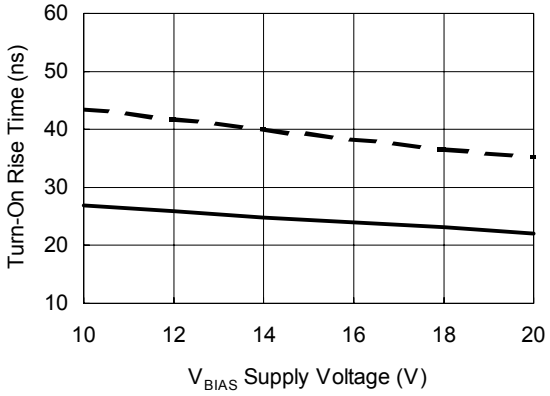


Figure 8B. Turn-On Rise Time vs. Supply Voltage

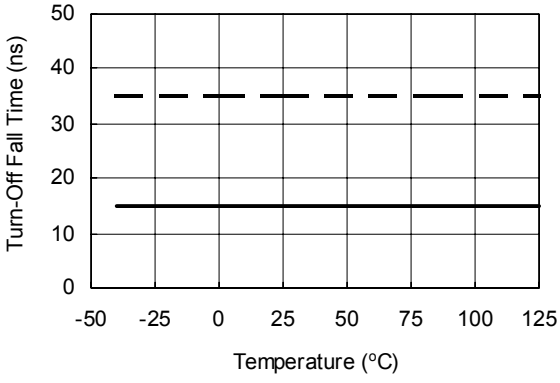


Figure 9A. Turn-Off Fall Time vs. Temperature

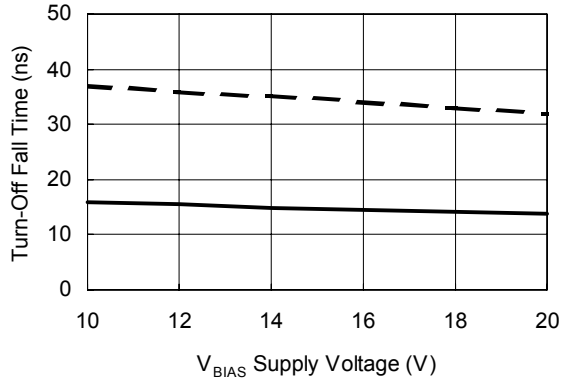


Figure 9B. Turn-Off Fall Time vs. Supply Voltage

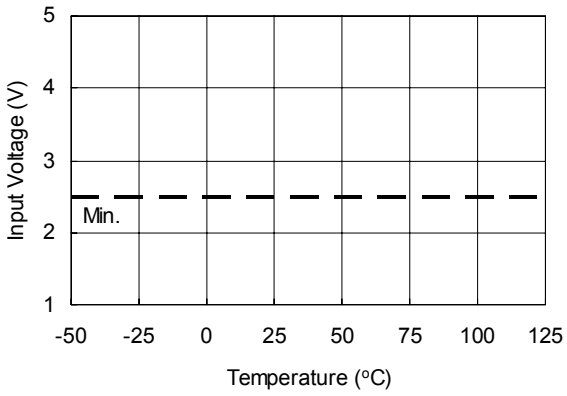


Figure 10A. Logic "1" Input Voltage vs. Temperature

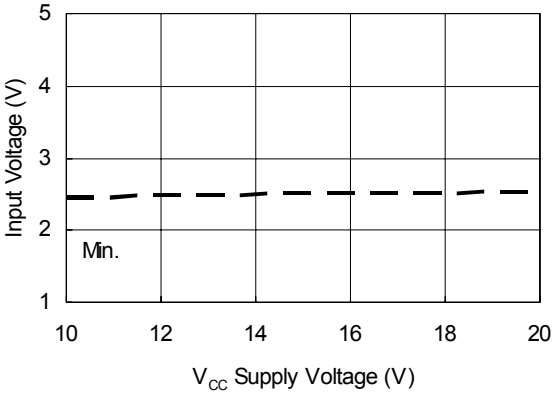


Figure 10B. Logic "1" Input Voltage vs. Supply Voltage

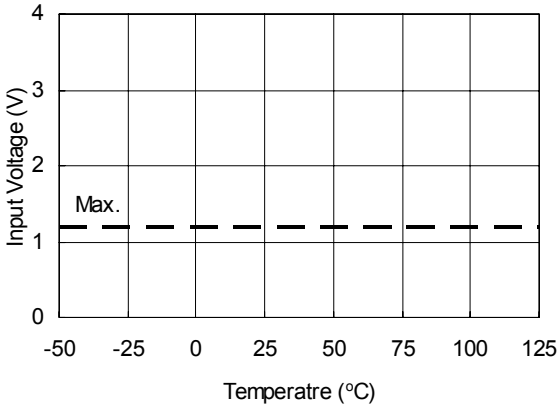


Figure 11A. Logic "0" Input Voltage vs. Temperature

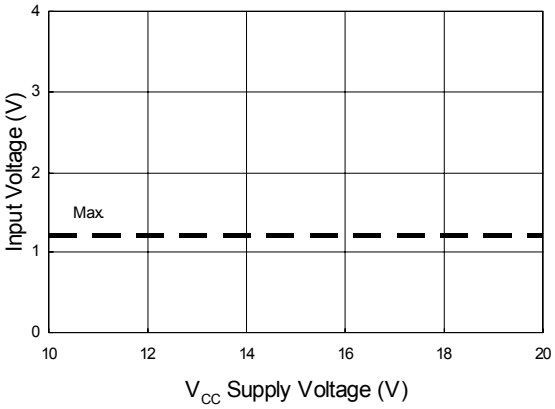


Figure 11B. Logic "0" Input Voltage vs. Supply Voltage

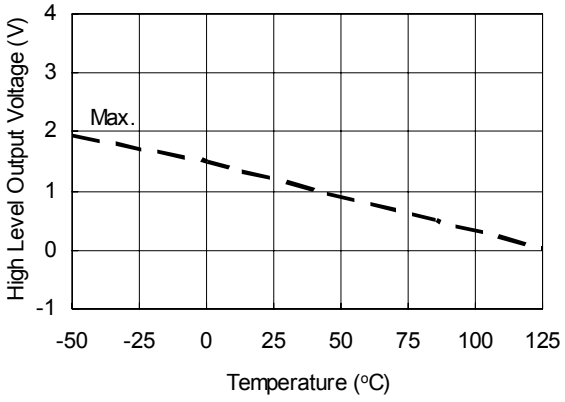


Figure 12A. High Level Output vs. Temperature

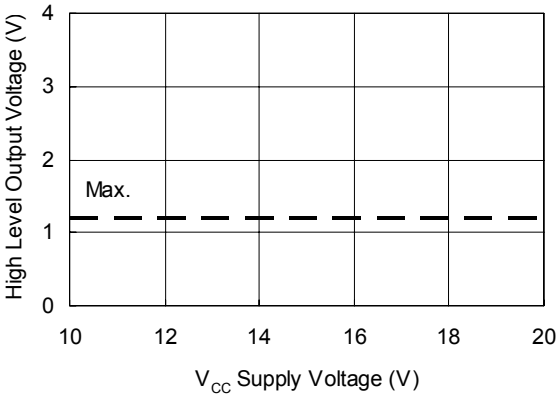


Figure 12B. High Level Output vs. Supply Voltage

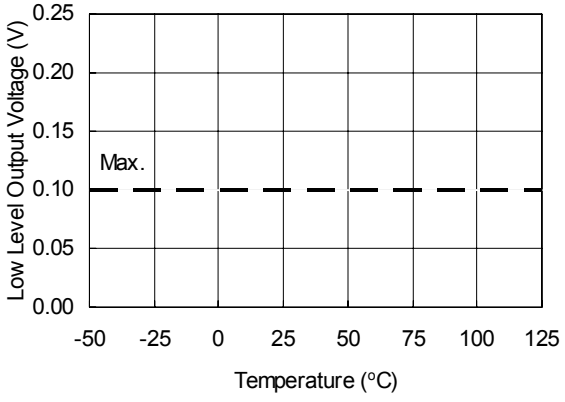


Figure 13A. Low Level Output vs.Temperature

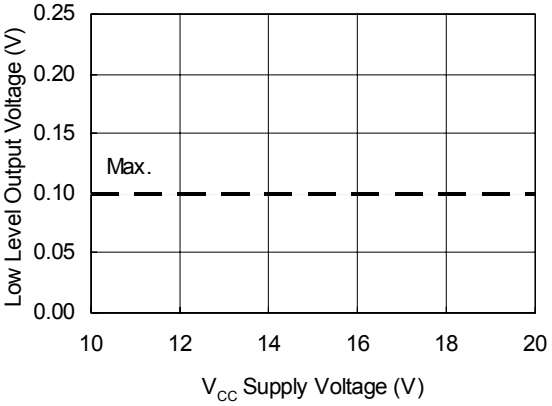


Figure 13B. Low Level Output vs. Supply Voltage

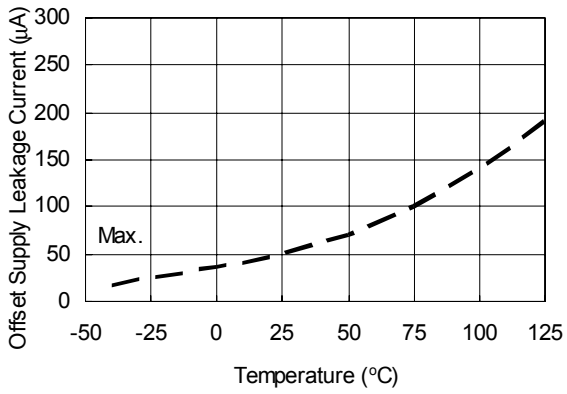


Figure 14A. Offset Supply Leakage Current vs. Temperature V_B=200v

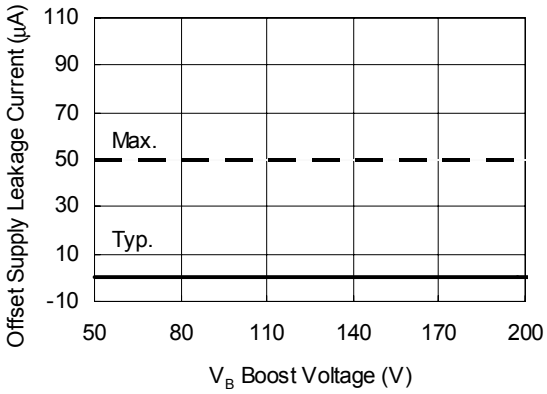


Figure 14B. Offset Supply Leakage Current vs. Supply Voltage

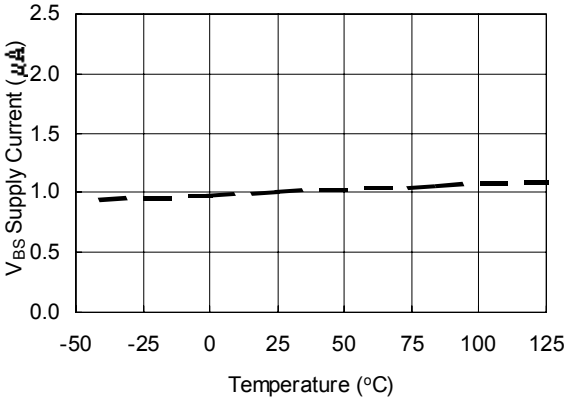


Figure 15A. V_{BS} Supply Current vs. Temperature

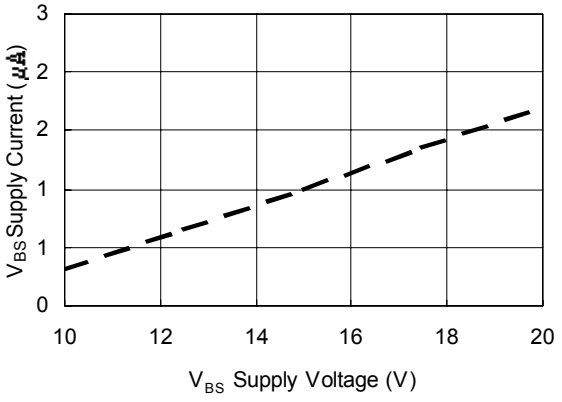


Figure 15B. V_{BS} Supply Current vs. Supply Voltage

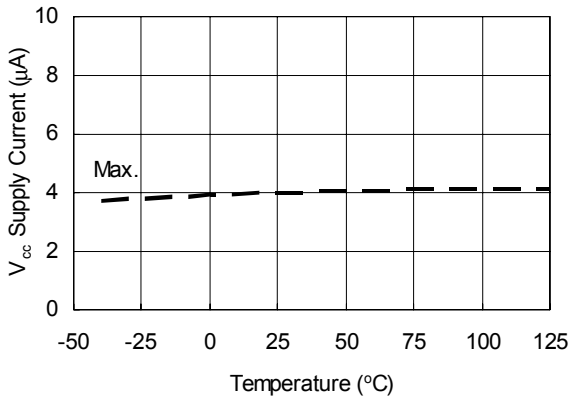


Figure 16A. V_{CC} Supply Current vs. Temperature

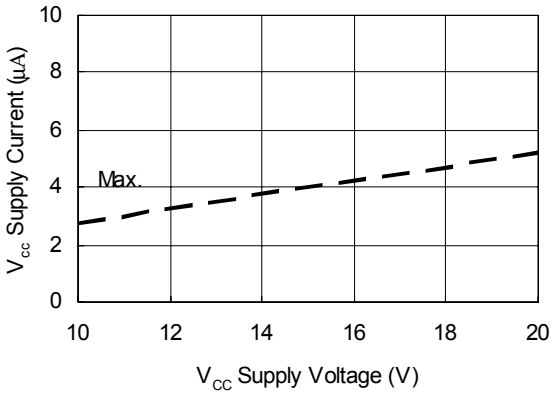


Figure 16B. V_{CC} Supply Current vs. Supply Voltage

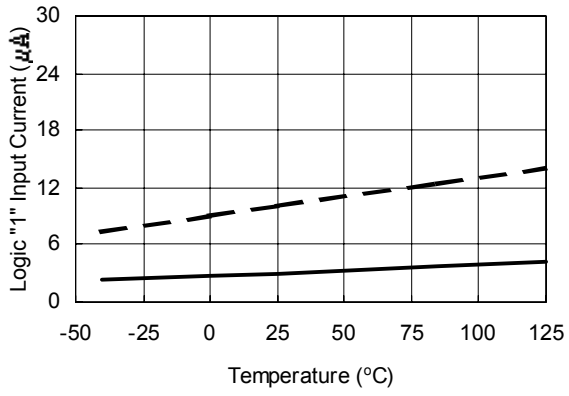


Figure 17A. Logic "1" Input Current vs. Temperature

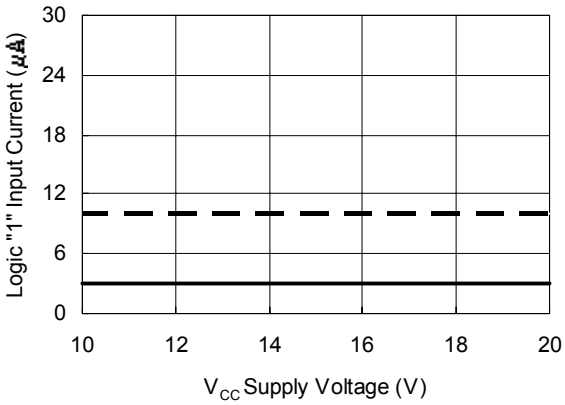


Figure 17B. Logic "1" Input Current vs. Supply Voltage

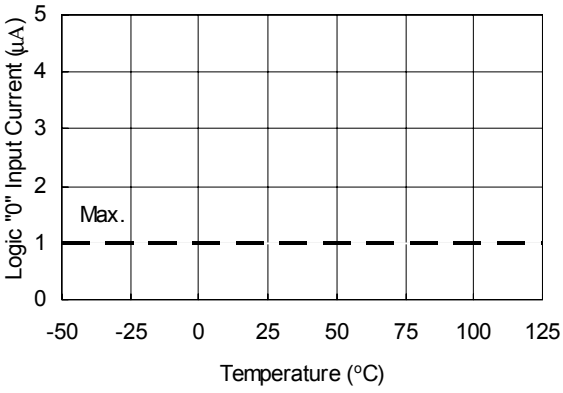


Figure 18A. Logic "0" Input Current vs. Temperature

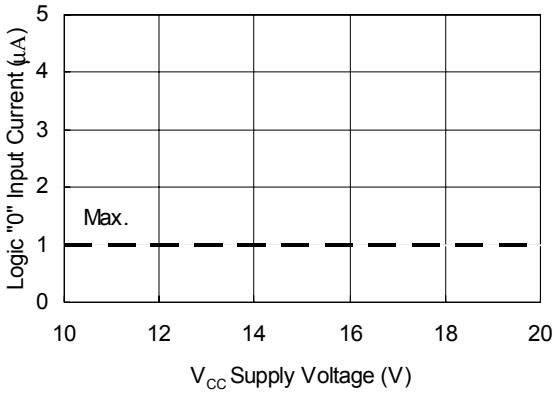


Figure 18B. Logic "0" Input Current vs. Supply Voltage

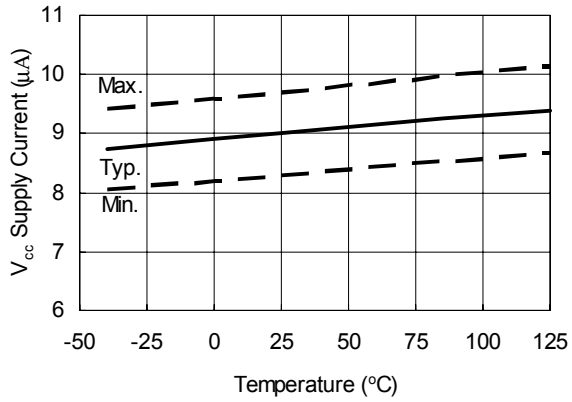


Figure 19. V_{cc} Undervoltage Threshold (+) vs. Temperature

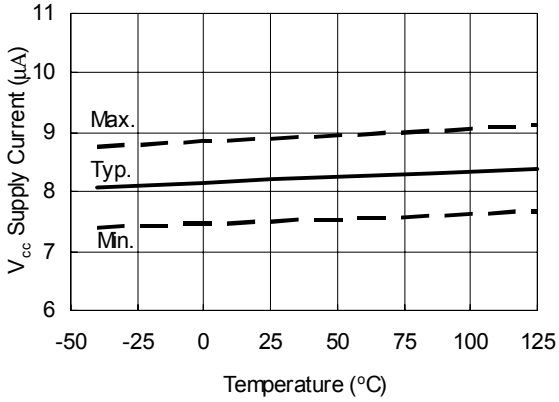


Figure 20. V_{cc} Undervoltage Threshold (-) vs. Temperature

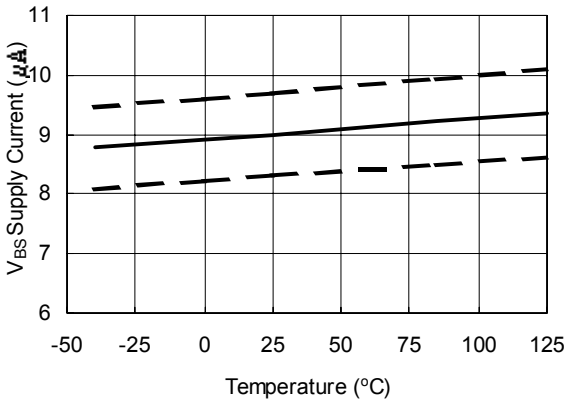


Figure 21. V_{BS} Undervoltage Threshold (+) vs. Temperature

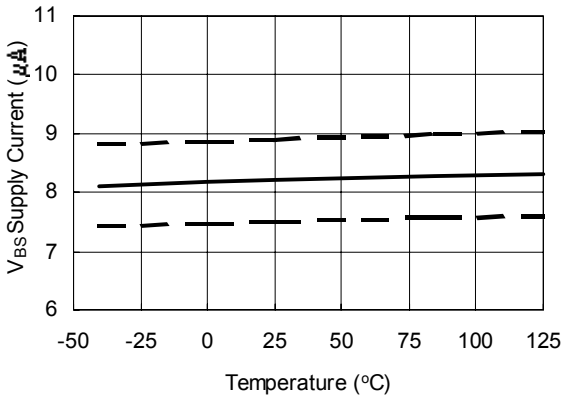


Figure 22. V_{BS} Undervoltage Threshold (-) vs. Temperature

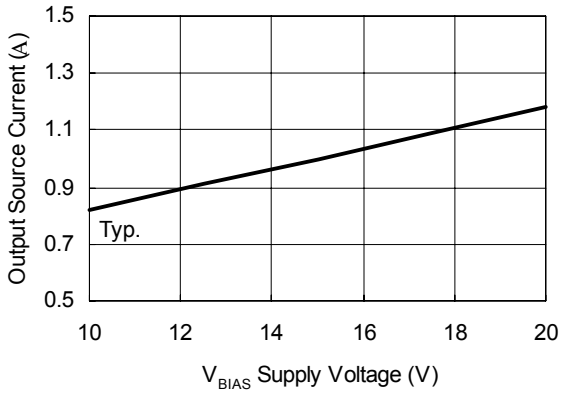


Figure 23. Output Source Current vs. Supply Voltage

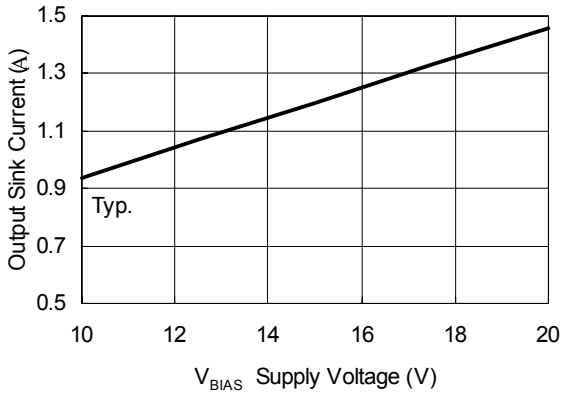


Figure 24. Output Sink Current vs. Supply Voltage

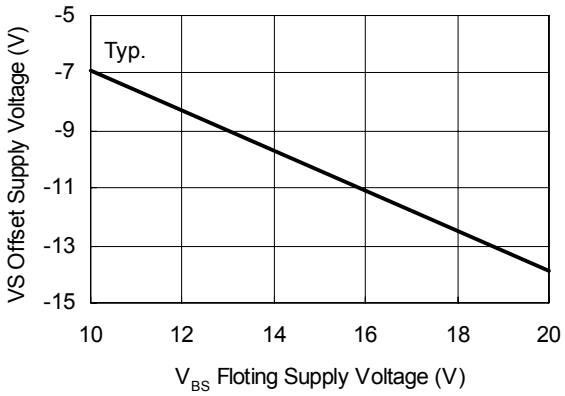


Figure 25. Maximum VS Negative Offset vs. Supply Voltage

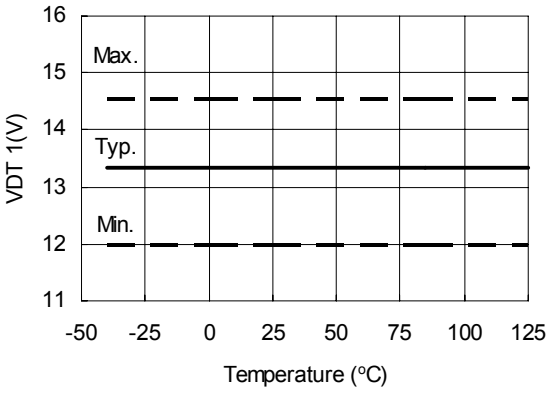


Figure 26. DT mode select Threshold (1) vs. Temperature

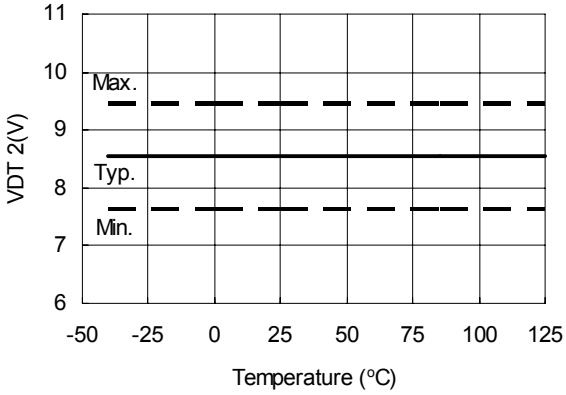


Figure 27. DT mode select Threshold (2) vs. Temperature

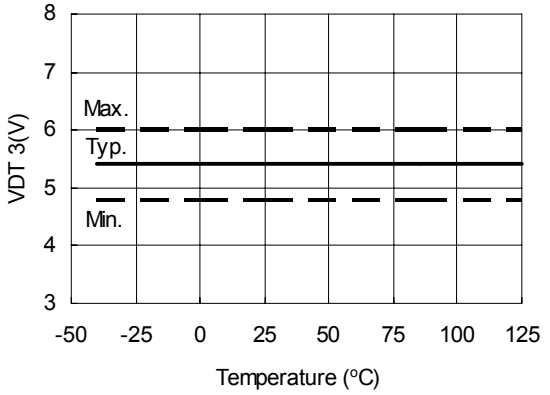


Figure 28. DT mode select Threshold (3) vs. Temperature

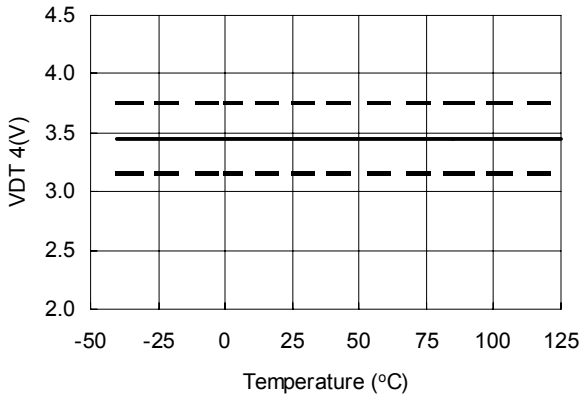


Figure 29. DT mode select Threshold (4) vs. Temperature

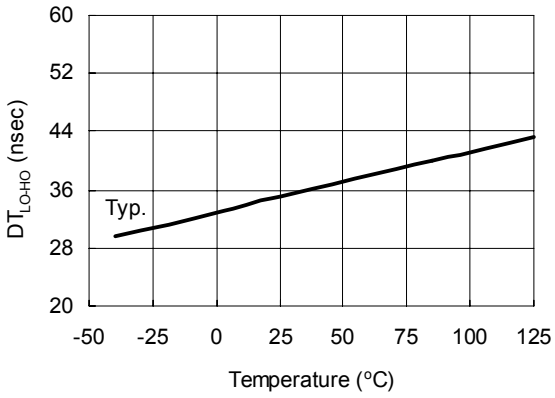


Figure 30. DT LO turn-off to HO turn-on (3) vs. Temperature

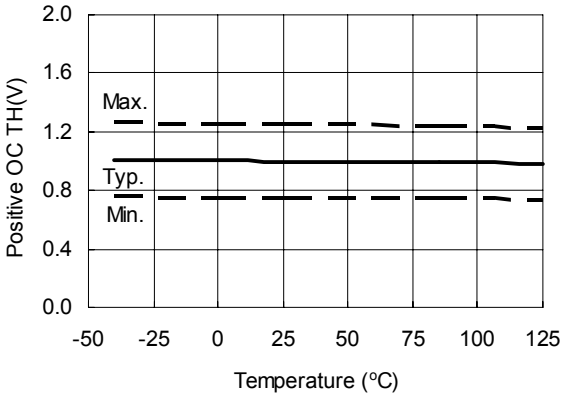


Figure 31. Positive OC Threshold(+) in VS vs. Temperature

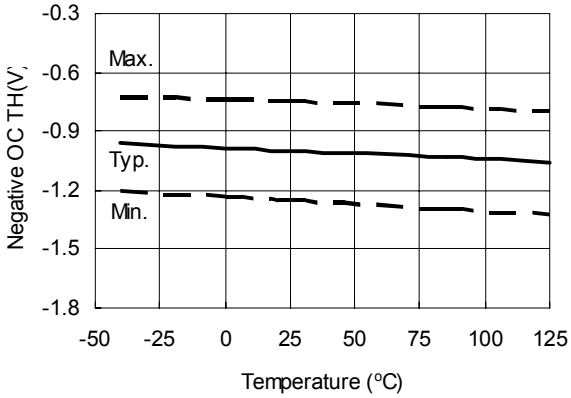


Figure 32. Negative OC Threshold(-) in VS vs. Temperature

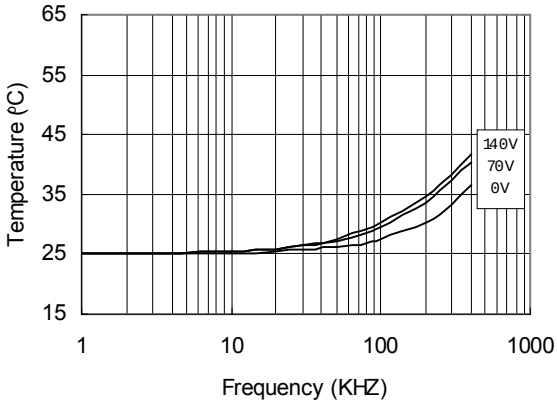


Figure 33. IRS20124s vs. Frequency (IRFBC20)
R_{gate}=33Ω, V_{CC}=12V

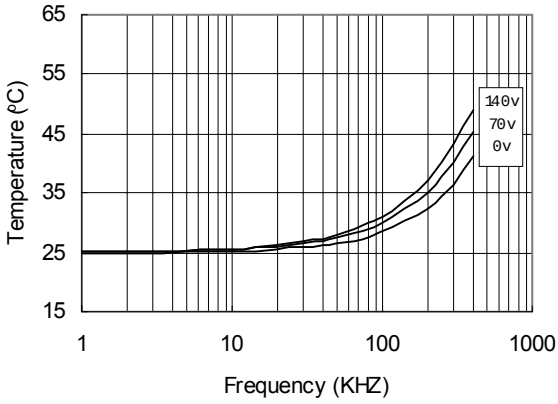


Figure 34. IRS20124s vs. Frequency (IRFBC30)
R_{gate}=22Ω, V_{CC}=12V

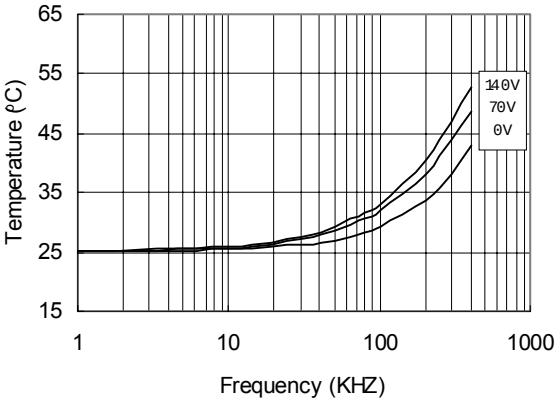


Figure 35. IRS20124s vs. Frequency (IRFBC40)
R_{gate}=15Ω, V_{CC}=12V

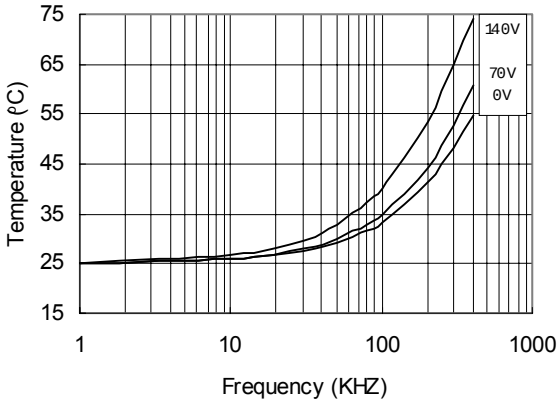


Figure 36. IRS20124s vs. Frequency (IRFPE50)
R_{gate}=10Ω, V_{CC}=12V

Functional description

Programmable Dead-time

The IRS20124 has an internal dead-time generation block to reduce the number of external components in the output stage of a Class D audio amplifier. Selectable dead-time through the DT/SD pin voltage is an easy and reliable function, which requires only two external resistors. The dead-time generation block is also designed to provide a constant dead-time interval, independent of Vcc fluctuations. Since the timings are critical to the audio performance of a Class D audio amplifier, the unique internal dead-time generation block is designed to be immune to noise on the DT/SD pin and the Vcc pin. Noise-free programmable dead-time function is available by selecting dead-time from four preset values, which are optimized and compensated.

How to Determine Optimal Dead-time

Please note that the effective dead-time in an actual application differs from the dead-time specified in this datasheet due to finite fall time, tf. The dead-time value in this datasheet is defined as the time period from the starting point of turn-off on one side of the switching stage to the starting point of turn-on on the other side as shown in Fig.5. The fall time of MOSFET gate voltage must be subtracted from the dead-time value in the datasheet to determine the effective dead time of a Class D audio amplifier.

(Effective dead-time)
= (Dead-time in datasheet) – (fall time, tf)

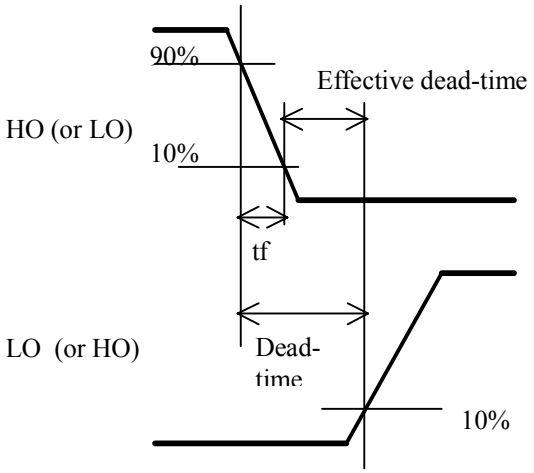


Figure 6. Effective Dead-time

A longer dead time period is required for a MOSFET with a larger gate charge value because of the longer tf. A shorter effective dead-time setting is always beneficial to achieve better linearity in the Class D switching stage. However, the likelihood of shoot-through current increases with narrower dead-time settings in mass production. Negative values of effective dead-time may cause excessive heat dissipation in the MOSFETs, potentially leading to their serious damage. To calculate the optimal dead-time in a given application, the fall time tf for both output voltages, HO and LO, in the actual circuit needs to be measured. In addition, the effective dead-time can also vary with temperature and device parameter variations. Therefore, a minimum effective dead-time of 10nS is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.

DT/SD pin

DT/SD pin provides two functions: 1) setting dead-time and 2) shutdown. The IRS20124 determines its operation mode based on the voltage applied to the DT/SD pin. An internal comparator translates which mode is being used by comparing internal reference voltages. Threshold voltages for each mode are set internally by a resistive voltage divider off Vcc, negating the need of using a precise absolute voltage to set the mode.

The relationship between the operation mode and the voltage at DT/SD pin is illustrated in the Fig.7.

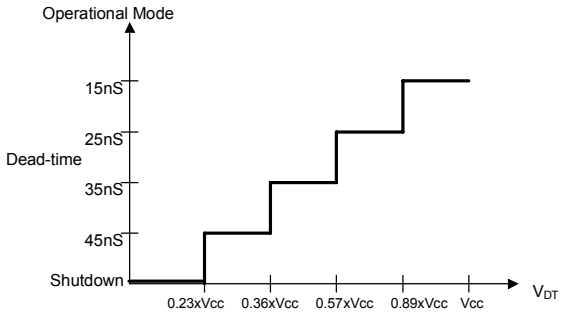


Figure 7. Dead-time Settings vs V_{DT} Voltage

Design Example

Table 1 shows suggested values of resistance for setting the dead-time. Resistors with up to 5% tolerance can be used if these listed values are followed.

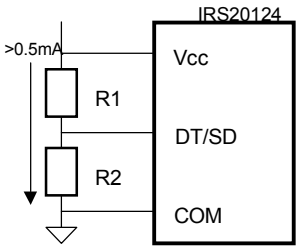


Figure 8. External Resistor

Dead-time mode	R1	R2	DT/SD voltage
DT1	<10k	Open	1.0 x Vcc
DT2	3.3k	8.2k	0.71 x Vcc
DT3	5.6k	4.7k	0.46 x Vcc
DT4	8.2k	3.3k	0.29 x Vcc

Table 1. Suggested resistor values for dead-time settings

Shutdown

Since IRS20124 has internal dead-time generation, independent inputs for HO and LO are no longer provided. Shutdown mode is the only way to turn off both MOSFETs simultaneously to protect them from over current conditions. If the DT/SD pin detects an input voltage below the threshold, $V_{DT4,}$ the IRS20124 will output 0V at both HO and LO outputs, forcing the switching output node to go into a high impedance state.

Over Current Sensing

In order to protect the power MOSFET, IRS20124 has a feature to detect over current conditions, which can occur when speaker wires are shorted together. The over current shutdown feature can be configured by combining the current sensing function with the shutdown mode via the DT/SD pin.

Load Current Direction in Class D Audio Application

In a Class D audio amplifier, the direction of the load current alternates according to the audio input signal. An over current condition can therefore happen during either a positive current cycle or a negative current cycle. Fig.9 shows the rela-

tionship between output current direction and the current in the low side MOSFET. It should be noted that each MOSFET carries a part of the load current in an audio cycle. Bi-directional current sensing offers over current detection capabilities in both cases by monitoring only the low side MOSFET.

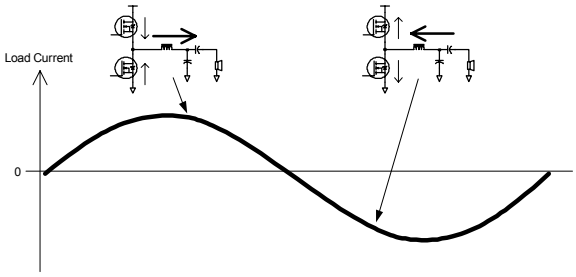


Figure 9. Direction in MMOSFET Current and Load Current

Bi-directional Current Sensing

IRS20124 has an over current detection function utilizing $R_{DS(ON)}$ of the low side switch as a current sensing shunt resistor. Due to the proprietary HVIC process, the IRS20124 is able to sense negative as well as positive current flow, enabling bi-directional load current sensing without the need for any additional external passive components.

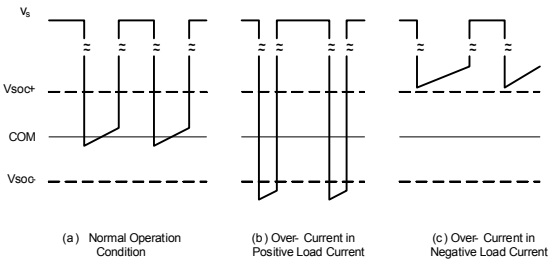


Figure 10. Vs Waveform in Over-current Condition

IRS20124 measures the current during the period when the low side MOSFET is turned on. Fig.10 illustrates how an excessive voltage at Vs node detects an over current condition. Under normal operating conditions, Vs voltage for the low side switch is well within the trip threshold boundaries, V_{SOC-} and $V_{SOC+.}$ In the case of Fig.9(b) which demonstrates the amplifier sourcing too much current to the load, the Vs node is found below the trip level, V_{SOC-}. In Fig.9(c) with opposite current direction, the amplifier sinks too much current from the load, positioning Vs well above trip level, $V_{SOC+.}$

Once the voltage in Vs exceeds the preset threshold, the OC pin pulls down to COM to detect an over current condition.

Since the switching waveform usually contains over/under shoot and associated oscillatory artifacts on their transient edges, a 200ns blanking interval is inserted in the Vs voltage sensing block at the instant the low side switch is engaged. Because of this blanking interval, the OC function will be unable to detect over current conditions if the low side ON duration less than 200ns.

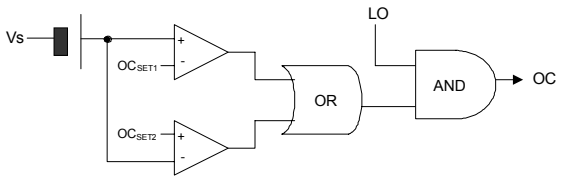


Figure 11. Simplified Functional Block Diagram of Bi-Directional Current Sensing

As shown in Fig.11, bi-directional current sensing block has an internal 2.0V level shifter feeding the signal to the comparator. OC_{SET1} sets the positive side threshold, and is given a trip level at V_{SOC+}, which is OC_{SET1} - 2.0V. In same way, for a given OC_{SET2}, V_{SOC-} is set at OC_{SET2} – 2.0V

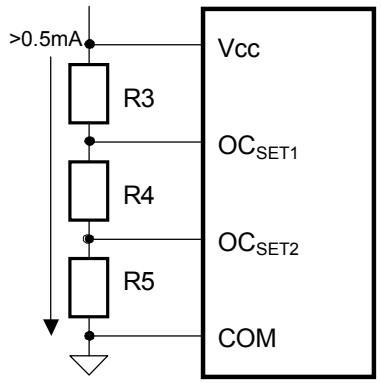


Figure 12. External Resistor Network to set OC Threshold

How to set OC Threshold

The positive and negative trip thresholds for bi-directional current sensing are set by the voltages at OC_{SET1} and OC_{SET2}. Fig.14 shows a typical resistor voltage divider that can. be used to set OC_{SET1} and OC_{SET2}.
The trip threshold voltages, V_{SOC+} and $V_{SOC+,}$ are determined by the required trip current levels, I_{TRIP+} and I_{TRIP-}, and $R_{DS(ON)}$ in the low side MOSFET.
Since the sensed voltage of Vs is shifted up by 2.21V internally and compared with the voltages fed to the OC_{SET1} and OC_{SET2} pins, the required value of OC_{SET1} with respect to COM is

$$V_{OCSET1} = V_{SOC+} + 2.21 = I_{TRIP+} \times R_{DS(ON)} + 2.21$$

The same relation holds between OC_{SET2} and $V_{SOC-,}$

$$V_{OCSET2} = V_{SOC-} + 2.21 = I_{TRIP-} \times R_{DS(ON)} + 2.21$$

In general, $R_{DS(ON)}$ has a positive temperature coefficient that needs to be considered when the threshold level is being set. Please also note that, in the negative load current direction, the sensing voltage at the Vs node is limited by the body diode of the low side MOSFET as explained later.

Design Example

This example demonstrates how to use the external? resistor network to set I_{TRIP+} and I_{TRIP-} to be ±11A, using a MOSFET that has $R_{DS(ON)}$ =60mΩ.

$V_{ISET1} = V_{TH}+ + 2.21 = I_{TRIP+} \times R_{DS(ON)} + 2.21 = 11 \times 60m\Omega + 2.21 = 2.87V$
$V_{ISET2} = V_{TH-} + 2.21 = I_{TRIP-} \times R_{DS(ON)} + 2.21 = (-11) \times 60m\Omega + 2.21 = 1.55V$

The total resistance of resistor network is based on the voltage at the Vcc and required bias current in this resistor network.

R_{total} =R3 + R4 + R5 = Vcc / I_{bias}
= 12V / 1mA = 12KΩ

The expected voltage across R3 is Vcc- V_{ISET1} = 12-2.87=9.13V. Similarly, the voltages across R4 is V_{SOC+} - V_{SOC-} = 2.87-1.55=1.32V, and the voltage across R5 is V_{ISET2}= 1.55V respectively.

R3 =9.13V/ I_{bias} = 9.13KΩ
R4 =1.32V/ I_{bias} = 1.32KΩ
R5 =1.55V/ I_{bias} = 1.55KΩ

Choose R3= 9.09KΩ, R4=1.33KΩ, R5=1.54KΩ from E-96 series.
Consequently, actual threshold levels are
V_{SOC+} =2.88V gives I_{TRIP+} = 11.2A
V_{SOC-} =1.55V gives I_{TRIP-} = -11.0A

Resisters with 1% tolerances are recommended.

OC Output Signal

The OC pin is a 20V open drain output. The OC pin is pulled down to ground when an over current condition is detected. A single external pull-up resistor can be shared by multiple IRS20124 OC pins to form the ORing logic. In order for a micro-processor to read the OC signal, this information is buffered with a mono stable multi vibrator to ensure 100ns minimum pulse width.
Because of unpredictable logic status of the OC pin, the OC signal should be ignored during power up/down.

Limitation from Body Diode in MOSFET

When a Class D stage outputs a positive current, flowing from the Class D amp to the load, the body diode of the MOSFET will turn on when the Drain to Source voltage of the MOSFET become larger than the diode forward drop voltage. In such a case, the sensing voltage at the Vs pin of the IRS20124 is clamped by the body diode. This means that the effective Rds(on) is now much lower than expected from Rds(on) of the MOSFET, and the Vs node my not able to reach the threshold to turn the OC output on before the MOSFET fails. Therefore, the region where body diode clamping takes a place should be avoided when setting V_{SOC-}.

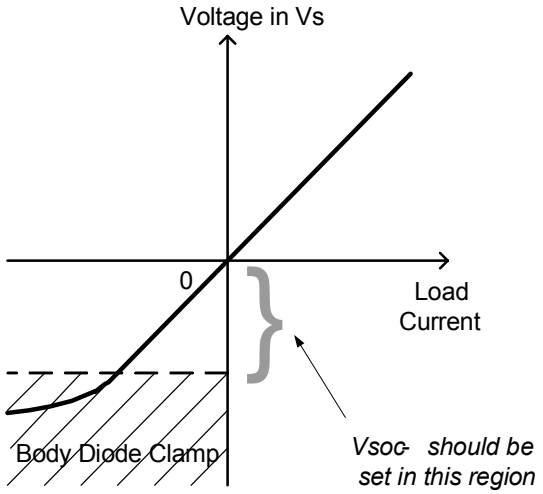


Figure 13. Body Diode in MOSFET Clamps vs Voltage

For further application information for gate driver IC please refer to AN-978 and DT98-2a. For further application information for class D application, please refer to AN-1070 and AN-1071.

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