
16 MHz STM8S 8-bit MCU, 8-Kbyte Flash memory, 128-byte data EEPROM, 10-bit ADC, 3 timers, UART, SPI, I2C

Datasheet - preliminary data

Features**Core**

- 16 MHz advanced STM8 core with Harvard architecture and 3-stage pipeline
- Extended instruction set

Memories

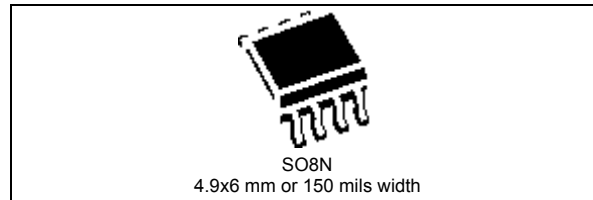
- Program memory: 8 Kbytes Flash memory; data retention 20 years at 55 °C after 100 cycles
- RAM: 1 Kbyte
- Data memory: 128-byte true data EEPROM; endurance up to 100 k write/erase cycles

Clock, reset and supply management

- 2.95 V to 5.5 V operating voltage
- Flexible clock control, 3 master clock sources
 - External clock input
 - Internal, user-trimmable 16 MHz RC
 - Internal low-power 128 kHz RC
- Clock security system with clock monitor
- Power management
 - Low-power modes (wait, active-halt, halt)
 - Switch-off peripheral clocks individually
 - Permanently active, low-consumption power-on and power-down reset

Interrupt management

- Nested interrupt controller with 32 interrupts
- Up to 5 external interrupts

**Timers**

- Advanced control timer: 16-bit, 2 CAPCOM channels, 2 outputs, dead-time insertion and flexible synchronization
- 16-bit general purpose timer, with 3 CAPCOM channels (IC, OC or PWM)
- 8-bit basic timer with 8-bit prescaler
- Auto wakeup timer
- Window and independent watchdog timers

Communications interfaces

- UART, SmartCard, IrDA, LIN master mode
- SPI unidirectional interface up to 8 Mbit/s (master simplex mode, slave receiver only)
- I2C interface up to 400 Kbit/s

Analog to digital converter (ADC)

- 10-bit ADC, ± 1 LSB ADC with up to 3 multiplexed channels, scan mode and analog watchdog

I/Os

- Up to 5 I/Os including 4 high-sink outputs
- Highly robust I/O design, immune against current injection

Development support

- Embedded single-wire interface module (SWIM) or fast on-chip programming and non-intrusive debugging

Contents

- 1 Introduction 8**
- 2 Description 9**
- 3 Block diagram 10**
- 4 Functional overview 11**
 - 4.1 Central processing unit STM8 11
 - 4.2 Single wire interface module (SWIM) and debug module (DM) 12
 - 4.3 Interrupt controller 12
 - 4.4 Flash program memory and data EEPROM 12
 - 4.5 Clock controller 15
 - 4.6 Power management 16
 - 4.7 Watchdog timers 16
 - 4.8 Auto wakeup counter 17
 - 4.9 TIM1 - 16-bit advanced control timer 17
 - 4.10 TIM2 - 16-bit general purpose timer 17
 - 4.11 TIM4 - 8-bit basic timer 17
 - 4.12 Analog-to-digital converter (ADC1) 18
 - 4.13 Communication interfaces 18
 - 4.13.1 UART1 18
 - 4.13.2 SPI 19
 - 4.13.3 I2C 19
- 5 Pinouts and pin descriptions 20**
 - 5.1 STM8S001J3 SO8N pinout and pin description 20
 - 5.2 Alternate function remapping 23
- 6 Memory and register map 24**
 - 6.1 Memory map 24
 - 6.2 Register map 25
 - 6.2.1 I/O port hardware register map 25
 - 6.2.2 General hardware register map 26

| | | | |
|-----------|--------|--|-----------|
| | 6.2.3 | CPU/SWIM/debug module/interrupt controller registers | 33 |
| 7 | | Interrupt vector mapping | 35 |
| 8 | | Option bytes | 36 |
| | 8.1 | Alternate function remapping bits | 38 |
| 9 | | Electrical characteristics | 39 |
| | 9.1 | Parameter conditions | 39 |
| | 9.1.1 | Minimum and maximum values | 39 |
| | 9.1.2 | Typical values | 39 |
| | 9.1.3 | Typical curves | 39 |
| | 9.1.4 | Loading capacitor | 39 |
| | 9.1.5 | Pin input voltage | 39 |
| | 9.2 | Absolute maximum ratings | 40 |
| | 9.3 | Operating conditions | 42 |
| | 9.3.1 | VCAP external capacitor | 44 |
| | 9.3.2 | Supply current characteristics | 44 |
| | 9.3.3 | External clock sources and timing characteristics | 53 |
| | 9.3.4 | Internal clock sources and timing characteristics | 53 |
| | 9.3.5 | Memory characteristics | 56 |
| | 9.3.6 | I/O port pin characteristics | 57 |
| | 9.3.7 | SPI serial peripheral interface | 65 |
| | 9.3.8 | I2C interface characteristics | 68 |
| | 9.3.9 | 10-bit ADC characteristics | 70 |
| | 9.3.10 | EMC characteristics | 73 |
| 10 | | Package information | 76 |
| | 10.1 | SO8N package information | 76 |
| | 10.2 | Thermal characteristics | 78 |
| | 10.2.1 | Reference document | 79 |
| | 10.2.2 | Selecting the product temperature range | 79 |
| 11 | | Ordering information | 80 |
| 12 | | STM8 development tools | 81 |
| | 12.1 | Emulation and in-circuit debugging tools | 81 |

| | | |
|-----------|---------------------------------|-----------|
| 12.2 | Software tools | 82 |
| 12.2.1 | STM8 toolset | 82 |
| 12.2.2 | C and assembly toolchains | 82 |
| 12.3 | Programming tools | 82 |
| 13 | Revision history | 83 |

List of tables

| | | |
|-----------|---|----|
| Table 1. | STM8S001J3 features | 9 |
| Table 2. | Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers | 15 |
| Table 3. | TIM timer features | 18 |
| Table 4. | Legend/abbreviations for STM8S001J3 pin description tables | 20 |
| Table 5. | STM8S001J3 pin description | 21 |
| Table 6. | Flash, Data EEPROM and RAM boundary addresses | 25 |
| Table 7. | I/O port hardware register map | 25 |
| Table 8. | General hardware register map | 27 |
| Table 9. | CPU/SWIM/debug module/interrupt controller registers | 33 |
| Table 10. | Interrupt mapping | 35 |
| Table 11. | Option bytes | 36 |
| Table 12. | Option byte description | 36 |
| Table 13. | STM8S001J3 alternate function remapping bits for 8-pin devices | 38 |
| Table 14. | Voltage characteristics | 40 |
| Table 15. | Current characteristics | 41 |
| Table 16. | Thermal characteristics | 41 |
| Table 17. | General operating conditions | 42 |
| Table 18. | Operating conditions at power-up/power-down | 43 |
| Table 19. | Total current consumption with code execution in run mode at $V_{DD} = 5\text{ V}$ | 44 |
| Table 20. | Total current consumption with code execution in run mode at $V_{DD} = 3.3\text{ V}$ | 45 |
| Table 21. | Total current consumption in wait mode at $V_{DD} = 5\text{ V}$ | 46 |
| Table 22. | Total current consumption in wait mode at $V_{DD} = 3.3\text{ V}$ | 46 |
| Table 23. | Total current consumption in active halt mode at $V_{DD} = 5\text{ V}$ | 47 |
| Table 24. | Total current consumption in active halt mode at $V_{DD} = 3.3\text{ V}$ | 47 |
| Table 25. | Total current consumption in halt mode at $V_{DD} = 5\text{ V}$ | 48 |
| Table 26. | Total current consumption in halt mode at $V_{DD} = 3.3\text{ V}$ | 48 |
| Table 27. | Wakeup times | 48 |
| Table 28. | Total current consumption and timing in forced reset state | 49 |
| Table 29. | Peripheral current consumption | 49 |
| Table 30. | HSE user external clock characteristics | 53 |
| Table 31. | HSI oscillator characteristics | 54 |
| Table 32. | LSI oscillator characteristics | 54 |
| Table 33. | RAM and hardware registers | 56 |
| Table 34. | Flash program memory and data EEPROM | 56 |
| Table 35. | I/O static characteristics | 57 |
| Table 36. | Output driving current (standard ports) | 59 |
| Table 37. | Output driving current (true open drain ports) | 59 |
| Table 38. | Output driving current (high sink ports) | 60 |
| Table 39. | SPI characteristics | 65 |
| Table 40. | I2C characteristics | 68 |
| Table 41. | ADC characteristics | 70 |
| Table 42. | ADC accuracy with $R_{AIN} < 10\text{ k}\Omega$, $V_{DD} = 5\text{ V}$ | 70 |
| Table 43. | ADC accuracy with $R_{AIN} < 10\text{ k}\Omega$, R_{AIN} , $V_{DD} = 3.3\text{ V}$ | 71 |
| Table 44. | EMS data | 73 |
| Table 45. | EMI data | 74 |
| Table 46. | ESD absolute maximum ratings | 74 |
| Table 47. | Electrical sensitivities | 75 |
| Table 48. | SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, | |

| | | |
|-----------|-------------------------------------|----|
| | package mechanical data | 76 |
| Table 49. | Thermal characteristics | 79 |
| Table 50. | Document revision history | 83 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | STM8S001J3 block diagram | 10 |
| Figure 2. | Flash memory organization | 13 |
| Figure 3. | STM8S001J3 SO8N pinout | 20 |
| Figure 4. | Memory map | 24 |
| Figure 5. | Pin loading conditions | 39 |
| Figure 6. | Pin input voltage | 40 |
| Figure 7. | f_{CPUmax} versus V_{DD} | 42 |
| Figure 8. | External capacitor C_{EXT} | 44 |
| Figure 9. | Typ. $I_{DD(RUN)}$ vs V_{DD} , HSE user external clock, $f_{CPU} = 16$ MHz | 50 |
| Figure 10. | Typ. $I_{DD(RUN)}$ vs f_{CPU} , HSE user external clock, $V_{DD} = 5$ V | 50 |
| Figure 11. | Typ. $I_{DD(RUN)}$ vs V_{DD} , HSI RC osc, $f_{CPU} = 16$ MHz | 51 |
| Figure 12. | Typ. $I_{DD(WFI)}$ vs. V_{DD} HSE user external clock, $f_{CPU} = 16$ MHz | 51 |
| Figure 13. | Typ. $I_{DD(WFI)}$ vs. f_{CPU} , HSE user external clock, $V_{DD} = 5$ V | 52 |
| Figure 14. | Typ. $I_{DD(WFI)}$ vs V_{DD} , HSI RC osc, $f_{CPU} = 16$ MHz | 52 |
| Figure 15. | HSE external clock source | 53 |
| Figure 16. | Typical HSI frequency variation vs V_{DD} at 4 temperatures | 54 |
| Figure 17. | Typical LSI frequency variation vs V_{DD} @ 4 temperatures | 55 |
| Figure 18. | Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures | 58 |
| Figure 19. | Typical pull-up resistance vs V_{DD} @ 4 temperatures | 58 |
| Figure 20. | Typical pull-up current vs V_{DD} @ 4 temperatures | 59 |
| Figure 21. | Typ. V_{OL} @ $V_{DD} = 5$ V (standard ports) | 60 |
| Figure 22. | Typ. V_{OL} @ $V_{DD} = 3.3$ V (standard ports) | 61 |
| Figure 23. | Typ. V_{OL} @ $V_{DD} = 5$ V (true open drain ports) | 61 |
| Figure 24. | Typ. V_{OL} @ $V_{DD} = 3.3$ V (true open drain ports) | 62 |
| Figure 25. | Typ. V_{OL} @ $V_{DD} = 5$ V (high sink ports) | 62 |
| Figure 26. | Typ. V_{OL} @ $V_{DD} = 3.3$ V (high sink ports) | 63 |
| Figure 27. | Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5$ V (standard ports) | 63 |
| Figure 28. | Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3$ V (standard ports) | 64 |
| Figure 29. | Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5$ V (high sink ports) | 64 |
| Figure 30. | Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3$ V (high sink ports) | 65 |
| Figure 31. | SPI timing diagram - slave mode and $CPHA = 0$ | 66 |
| Figure 32. | SPI timing diagram - slave mode and $CPHA = 1^{(1)}$ | 67 |
| Figure 33. | SPI timing diagram - master mode ⁽¹⁾ | 67 |
| Figure 34. | Typical application with I2C bus and timing diagram | 69 |
| Figure 35. | ADC accuracy characteristics | 72 |
| Figure 36. | Typical application with ADC | 72 |
| Figure 37. | SO8N – 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package outline | 76 |
| Figure 38. | SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, package recommended footprint | 77 |
| Figure 39. | SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, marking example | 78 |
| Figure 40. | STM8S001J3 ordering information scheme ⁽¹⁾ | 80 |

1 Introduction

This datasheet contains the description of the STM8S001J3 features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S and STM8A microcontroller families reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the PM0051 (How to program STM8S and STM8A Flash program memory and data EEPROM).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8S001J3 8-bit microcontrollers offer 8 Kbytes of Flash program memory, plus integrated true data EEPROM. It is referred to as low-density device in the STM8S microcontroller family reference manual (RM0016).

The STM8S001J3 device provides the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by true data EEPROM supporting up to 100000 write/erase cycles, advanced core and peripherals made in a state-of-the-art technology at 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

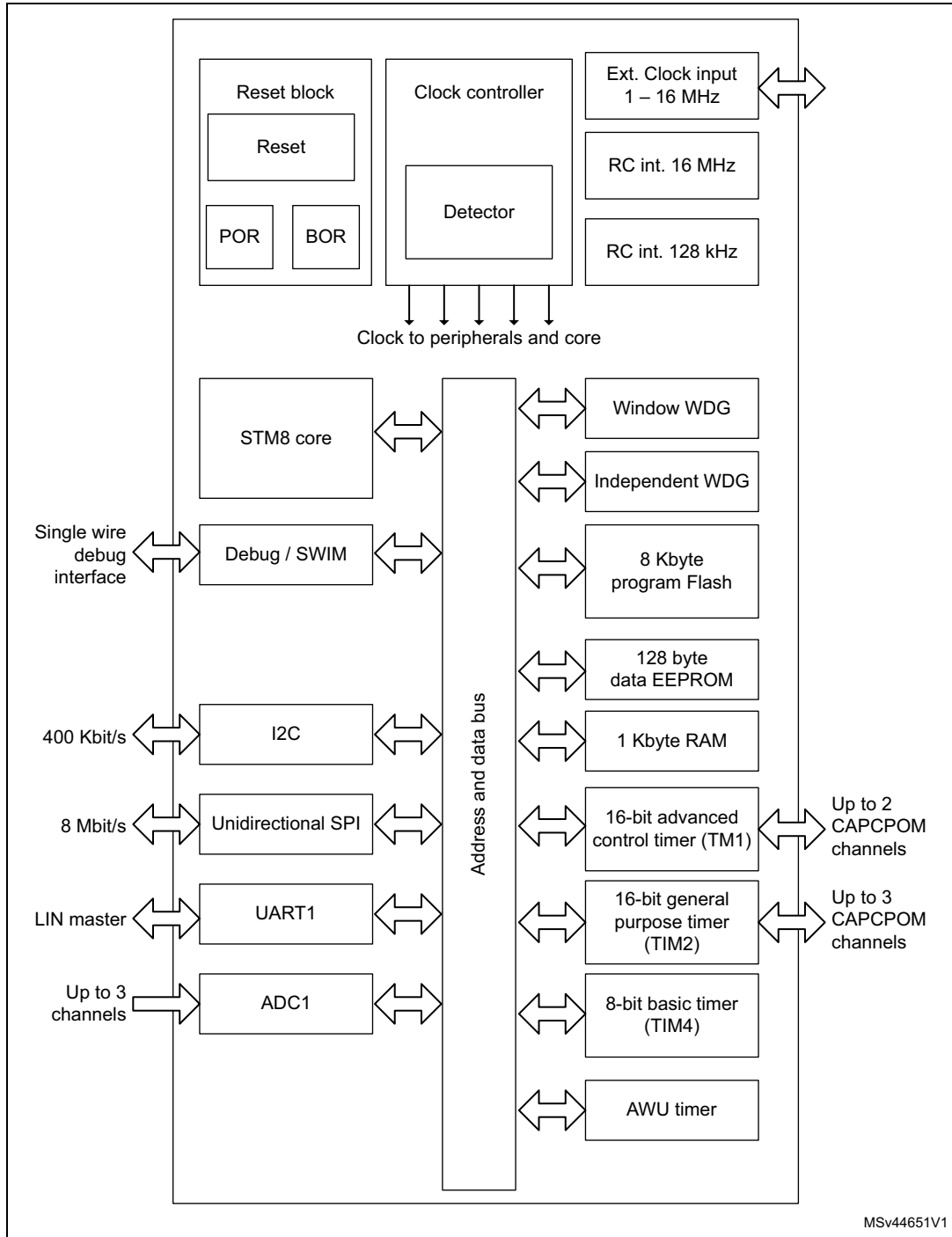
Table 1. STM8S001J3 features

| Features | STM8S001J3 |
|---|---|
| Pin count | 8 |
| Max. number of GPIOs (I/O) | 5 |
| External interrupt pins | 5 |
| Timer CAPCOM channels | 3 |
| Timer complementary outputs | 1 |
| A/D converter channels | 3 |
| High-sink I/Os | 4 |
| Low-density Flash program memory (byte) | 8 K |
| RAM (byte) | 1 K |
| True data EEPROM (byte) | 128 ⁽¹⁾ |
| Peripheral set | Multi purpose timer (TIM1), SPI unidirectional, I2C, UART, Window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4) |

1. Without read-while-write capability.

3 Block diagram

Figure 1. STM8S001J3 block diagram



MSv44651V1

4 Functional overview

The following section intends to give an overview of the basic features of the STM8S001J3 functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 byte/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

Recommendation for SWIM pin (pin #8) sharing

As the NRST pin is not available on this device, if the SWIM pin should be used with the I/O pin functionality, it is recommended to add a ~5 seconds delay in the firmware before changing the functionality on the pin with SWIM functions. This action allows the user to set the device into SWIM mode after the device power on and to be able to reprogram the device. If the pin with SWIM functionality is set to I/O mode immediately after the device reset, the device is unable to connect through the SWIM interface and it gets locked forever. This initial delay can be removed in the final (locked) code.

4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 5 external interrupts including TLI
- Trap and reset interrupts

4.4 Flash program memory and data EEPROM

- 8 Kbytes of Flash program single voltage Flash memory
- 128 byte true data EEPROM
- User option byte area

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to modify the content of main program memory and data EEPROM, or to reprogram the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to [Figure 2](#).

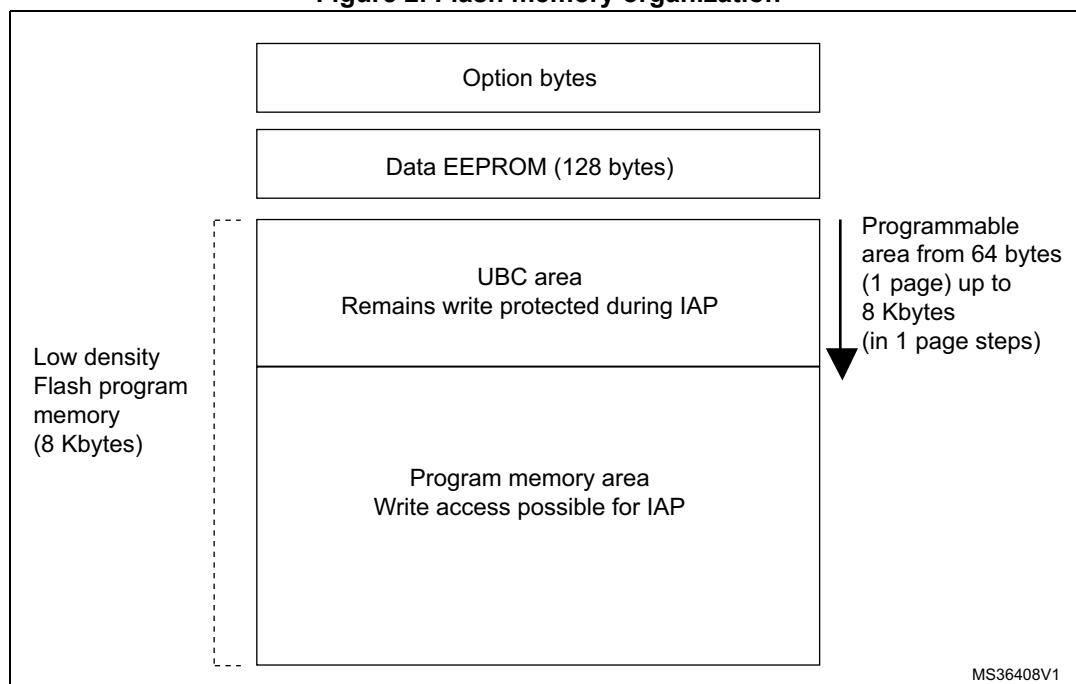
The size of the UBC is programmable through the UBC option byte ([Table 12](#)), in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

Recommendation for the device's programming:

The device's 8 Kbytes program memory is not empty on virgin devices; there is code loop implemented on the reset vector. It is recommended to keep valid code loop in the device to avoid the program execution from an invalid memory address (which would be any memory address out of 8 Kbytes program memory space).

If the device's program memory is empty (0x00 content), it displays the behavior described below:

- After the power on, the “empty” code is executed (0x0000 opcodes = instructions: NEG (0x00, SP)) until the device reaches the end of the 8 Kbytes program memory (the end address = 0x9FFF).
It takes around 4 milliseconds to reach the end of the 8 Kbytes memory space @2 MHz HSI clock.
- Once the device reaches the end of the 8 Kbytes program memory, the program continues and code from a non-existing memory is fetched and executed.
The reading of non-existing memory is a random content which can lead to the execution of invalid instructions.
The execution of invalid instructions generates a software reset and the program starts again. A reset can be generated every 4 milliseconds or more.

Only the “connect on-the-fly” method can be used to program the device through the SWIM interface. The “connect under-reset” method cannot be used because the NRST pin is not available on this device.

The “connect on-the-fly” mode can be used while the device is executing code, but if there is a device reset (by software reset) during the SWIM connection, this connection is aborted and it must be performed again from the debug tool. Note that the software reset occurrence can be of every 4 milliseconds, making it difficult to successfully connect to the device's debug tool (there is practically only one successful connection trial for every 10 attempts). Once that a successful connection is reached, the device can be programmed with a valid firmware without problems; therefore it is recommended that device is never erased and that it contains always a valid code loop.

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** Three different clock sources can be used to drive the master clock:
 - Up to 16 MHz high-speed user-external clock (HSE user-ext)
 - 16 MHz high-speed internal RC oscillator (HSI)
 - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

| Bit | Peripheral clock | Bit | Peripheral clock | Bit | Peripheral clock | Bit | Peripheral clock |
|---------|------------------|---------|------------------|---------|------------------|---------|------------------|
| PCKEN17 | TIM1 | PCKEN13 | UART1 | PCKEN27 | Reserved | PCKEN23 | ADC |
| PCKEN16 | Reserved | PCKEN12 | Reserved | PCKEN26 | Reserved | PCKEN22 | AWU |
| PCKEN15 | TIM2 | PCKEN11 | SPI | PCKEN25 | Reserved | PCKEN21 | Reserved |
| PCKEN14 | TIM4 | PCKEN10 | I2C | PCKEN24 | Reserved | PCKEN20 | Reserved |

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between the lowest power consumption, the fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode:** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: at 16 MHz CPU clock the time-out period can be adjusted between 75 μ s up to 64 ms.
2. Refresh out of window: the down-counter is refreshed before its value is lower than the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 μ s to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration

4.9 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- One complementary output (CH1 with CH1N option) with adjustable dead time
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.10 TIM2 - 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1...32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update

4.11 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. TIM timer features

| Timer | Counter size (bits) | Prescaler | Counting mode | CAPCOM channels | Complem. outputs | Ext. trigger | Timer synchronization/chaining |
|-------|---------------------|--------------------------------|---------------|-----------------|------------------|--------------|--------------------------------|
| TIM1 | 16 | Any integer from 1 to 65536 | Up/down | 2 | 1 ⁽¹⁾ | No | No |
| TIM2 | 16 | Any power of 2 from 1 to 32768 | Up | 3 | 0 | No | |
| TIM4 | 8 | Any power of 2 from 1 to 128 | Up | 0 | 0 | No | |

1. TIM1_CH2N with TIM1_CH1

4.12 Analog-to-digital converter (ADC1)

STM8S001J3 contains a 10-bit successive approximation A/D converter (ADC1) with up to three external multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous, buffered continuous conversion modes
- Buffer size (10 x 10 bits)
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.13 Communication interfaces

The following communication interfaces are implemented:

- UART1: full feature UART, synchronous mode, SmartCard mode, IrDA mode, LIN2.1 master capability
- SPI: master mode transmit/receive only, slave mode receive only, 8 Mbit/s
- I²C: up to 400 Kbit/s

4.13.1 UART1

Main features

- 1 Mbit/s full duplex SCI
- High precision baud rate generator
- Smartcard reader emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s ($f_{CPU}/16$) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
 - Address bit (MSB)
 - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master mode

- Emission: generates 13-bit synch. break frame
- Reception: detects 11-bit break frame

4.13.2 SPI

- Maximum speed: 8 Mbit/s ($f_{MASTER}/2$) both for master and slave
- Unidirectional transfer: SPI master mode transmit/receive only, SPI slave mode receive only
- Simplex master synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by software
- CRC calculation
- 1 byte Tx and Rx buffer

4.13.3 I2C

- I2C master features
 - Clock generation
 - Start and stop generation
- I2C slave features
 - Programmable I2C address detection
 - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds
 - Standard speed (up to 100 kHz)
 - Fast speed (up to 400 kHz)

5 Pinouts and pin descriptions

This section presents the pinouts and pin descriptions for STM8S001J3. [Table 4](#) introduces the legends and abbreviations that are used in the upcoming subsections.

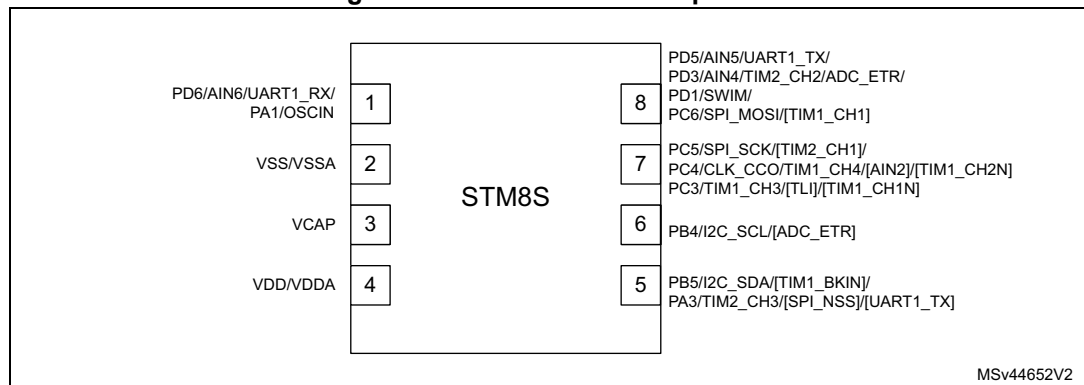
Table 4. Legend/abbreviations for STM8S001J3 pin description tables

| | | |
|--------------------------------|---|--|
| Type | I = input, O = output, S = power supply | |
| Level | Input | CM = CMOS |
| | Output | HS = high sink |
| Output speed | O1 = slow (up to 2 MHz) O2 = fast (up to 10 MHz) O3 = fast/slow programmability with slow as default state after reset O4 = fast/slow programmability with fast as default state after reset | |
| Port and control configuration | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push pull |
| Reset state | Bold x (pin state after internal reset release) Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release. | |

5.1 STM8S001J3 SO8N pinout and pin description

[Figure 3](#) presents the STM8S001J3 pinout image and [Table 5](#) below presents the device's pins description.

Figure 3. STM8S001J3 SO8N pinout



1. [] Alternative function option (if the same alternate function is shown twice, it indicated an exclusive choice and not a duplication of the function).

Table 5. STM8S001J3 pin description

| Pin no. | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---------|--|------|----------|-----|--------------|--------------------------|-------|------------------|----|-----------------------------|---|---|
| | | | floating | wpu | Ext. interr. | High sink ⁽¹⁾ | Speed | OD | PP | | | |
| 1 | PD6/ AIN6/ UART1_RX | I/O | X | X | X | HS | O3 | X | X | Port D6 | Analog input 6/ UART1 data receive | - |
| | PA1/ OSCIN ⁽²⁾ | I/O | X | X | X | - | O1 | X | X | Port A1 | External clock input (HSE clock) | - |
| 2 | VSS/VSSA | S | - | - | - | - | - | - | - | Ground | | - |
| 3 | VCAP | S | - | - | - | - | - | - | - | 1.8 V regulator capacitor | | - |
| 4 | VDD/VDDA | S | - | - | - | - | - | - | - | Power supply | | - |
| 5 | PA3/ TIM2_CH3 [SPI_NSS] \ [UART1_TX] | I/O | X | X | X | HS | O3 | X | X | Port A3 | Timer 2 channel 3 | SPI master/ slave select [AFR1] UART1 data transmit [AFR1 and AFR0] |
| | PB5/ I2C_SDA [TIM1_BKIN] | I/O | X | - | X | - | O1 | T ⁽³⁾ | - | Port B5 | I2C data | Timer 1 - break input [AFR4] |
| 6 | PB4/ I2C_SCL / [ADC_ETR] | I/O | X | - | X | - | O1 | T ⁽³⁾ | - | Port B4 | I2C clock | ADC external trigger [AFR4] |
| 7 | PC3/ TIM1_CH3 [TLI] [TIM1_CH1N] | I/O | X | X | X | HS | O3 | X | X | Port C3 | Timer 1 - channel 3 | Top level interrupt [AFR3] Timer 1 - inverted channel 1 [AFR7] |
| | PC4/ CLK_CCO/ TIM1_CH4/[AIN2]/ [TIM1_CH2N] | I/O | X | X | X | HS | O3 | X | X | Port C4 | Configurable clock output/Timer 1 - channel 4 | Analog input 2 [AFR2], Timer 1 - inverted channel 2 [AFR7] |
| | PC5/ SPI_SCK [TIM2_CH1] | I/O | X | X | X | HS | O3 | X | X | Port C5 | SPI clock | Timer 2 - channel 1 [AFR0] |

Table 5. STM8S001J3 pin description (continued)

| Pin no. | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---------|------------------------------|------|------------------|------------------|--------------|--------------------------|-------|----|----|-----------------------------|--|---|
| | | | floating | wpu | Ext. interr. | High sink ⁽¹⁾ | Speed | OD | PP | | | |
| 8 | PC6/ SPI_MOSI [TIM1_CH1] | I/O | X ⁽⁴⁾ | X | X | HS | O3 | X | X | Port C6 | SPI master out/slave in | Timer 1 - channel 1 [AFR0] |
| | PD1/ SWIM ⁽⁴⁾ | I/O | X | X ⁽⁴⁾ | X | HS | O4 | X | X | Port D1 | SWIM data interface | - |
| | PD3/ AIN4/ TIM2_CH2/ ADC_ETR | I/O | X ⁽⁴⁾ | X | X | HS | O3 | X | X | Port D3 | Analog input 4/ Timer 2 - channel 2/ADC external trigger | - |
| | PD5/ AIN5/ UART1_TX | I/O | X ⁽⁴⁾ | X | X | HS | O3 | X | X | Port D5 | Analog input 5/ UART1 data transmit | - |

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented). Although PB5 itself is a true open drain GPIO with its respective internal circuitry and characteristics, V_{IN} maximum of the pin number 5 is limited by the standard GPIO PA3 which is also bonded to pin number 5.
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release. This PD1 default state influences all GPIOs connected in parallel on pin# 8 (PC6, PD3, PD5).

Note: The PA2, PB0, PB1, PB2, PB3, PB6, PB7, PC1, PC2, PC7, PD0, PD2, PD4, PD7, PE5 and PF4 GPIOs should be configured after device reset in output push-pull mode with output low-state to reduce the device's consumption and to improve its EMC immunity. The GPIOs mentioned above are not connected to pins, and they are in input-floating mode after a device reset.

Note: As several pins provide a connection to multiple GPIOs, the mode selection for any of those GPIOs impacts all the other GPIOs connected to the same pin. The user is responsible for the proper setting of the GPIO modes in order to avoid conflicts between GPIOs bonded to the same pin (including their alternate functions). For example, pull-up enabled on PD1 is also seen on PC6, PD3 and PD5. Push-pull configuration of PC3 is also seen on PC4 and PC5, etc.

5.2 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to [Section 8: Option bytes](#). When the remapping option is active, the default alternate function is no longer available.

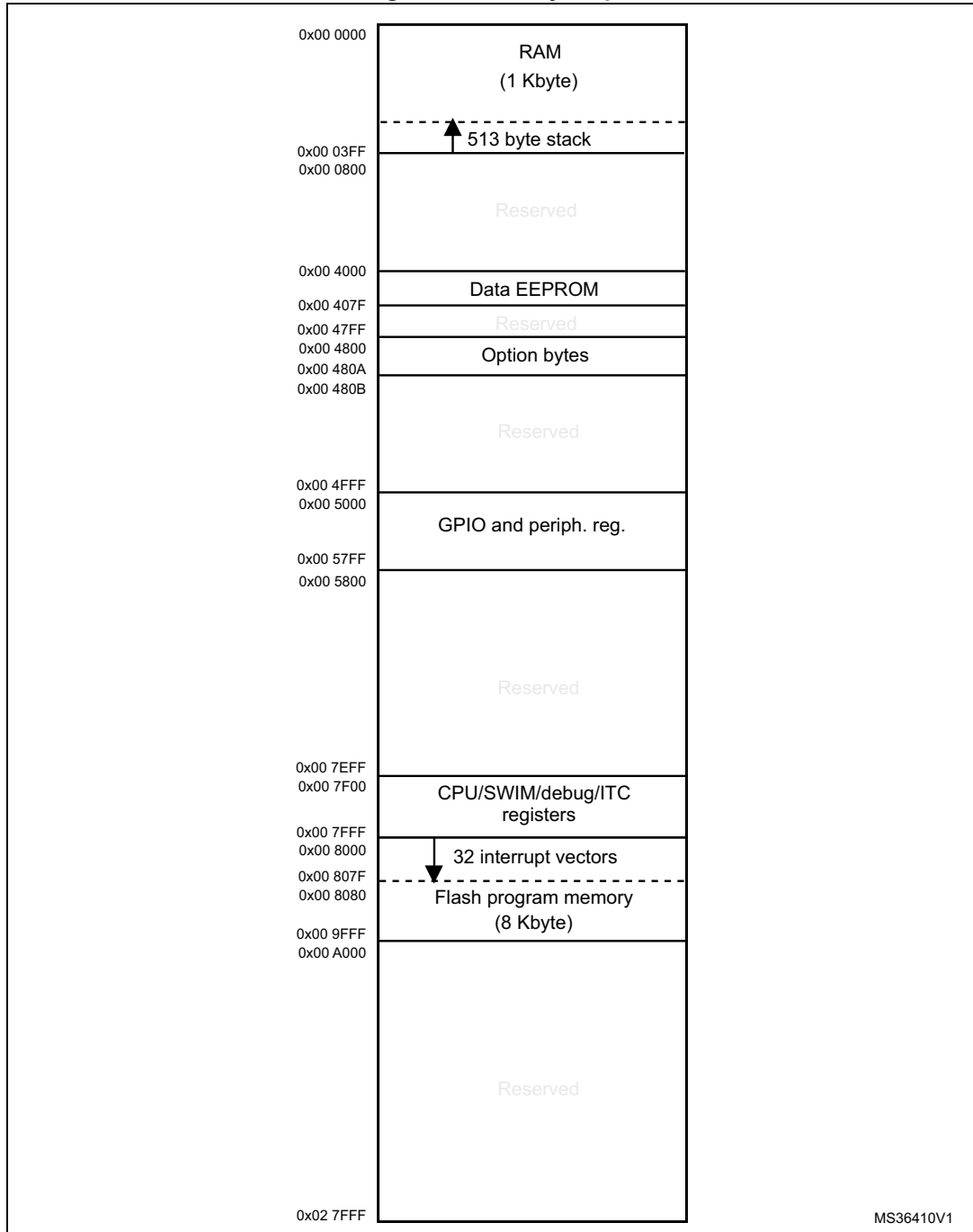
To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

6 Memory and register map

6.1 Memory map

Figure 4. Memory map



MS36410V1

Table 6 lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 6. Flash, Data EEPROM and RAM boundary addresses

| Memory area | Size (byte) | Start address | End address |
|----------------------|-------------|---------------|-------------|
| Flash program memory | 8 K | 0x00 8000 | 0x00 9FFF |
| RAM | 1 K | 0x00 0000 | 0x00 03FF |
| Data EEPROM | 128 | 0x00 4000 | 0x00 407F |

6.2 Register map

6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

| Address | Block | Register label | Register name | Reset status |
|-----------|--------|----------------|-----------------------------------|---------------------|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xXX ⁽¹⁾ |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x00 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xXX ⁽¹⁾ |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PC_IDR | Port C input pin value register | 0xXX ⁽¹⁾ |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xXX ⁽¹⁾ |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x02 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |

Table 7. I/O port hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|-----------|--------|----------------|-----------------------------------|---------------------|
| 0x00 5014 | Port E | PE_ODR | Port E data output latch register | 0x00 |
| 0x00 5015 | | PE_IDR | Port E input pin value register | 0xXX ⁽¹⁾ |
| 0x00 5016 | | PE_DDR | Port E data direction register | 0x00 |
| 0x00 5017 | | PE_CR1 | Port E control register 1 | 0x00 |
| 0x00 5018 | | PE_CR2 | Port E control register 2 | 0x00 |
| 0x00 5019 | Port F | PF_ODR | Port F data output latch register | 0x00 |
| 0x00 501A | | PF_IDR | Port F input pin value register | 0xXX ⁽¹⁾ |
| 0x00 501B | | PF_DDR | Port F data direction register | 0x00 |
| 0x00 501C | | PF_CR1 | Port F control register 1 | 0x00 |
| 0x00 501D | | PF_CR2 | Port F control register 2 | 0x00 |

1. Depends on the external circuitry.

6.2.2 General hardware register map

Table 8. General hardware register map

| Address | Block | Register label | Register name | Reset status |
|------------------------|-------------------------|----------------|--|---------------------|
| 0x00 501E to 0x00 5059 | Reserved area (60 byte) | | | |
| 0x00 505A | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 505B | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 505C | | FLASH_NCR2 | Flash complementary control register 2 | 0xFF |
| 0x00 505D | | FLASH_FPR | Flash protection register | 0x00 |
| 0x00 505E | | FLASH_NFPR | Flash complementary protection register | 0xFF |
| 0x00 505F | | FLASH_IAPSR | Flash in-application programming status register | 0x00 |
| 0x00 5060 to 0x00 5061 | Reserved area (2 byte) | | | |
| 0x00 5062 | Flash | FLASH_PUKR | Flash Program memory unprotection register | 0x00 |
| 0x00 5063 | Reserved area (1 byte) | | | |
| 0x00 5064 | Flash | FLASH_DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5065 to 0x00 509F | Reserved area (59 byte) | | | |
| 0x00 50A0 | ITC | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 to 0x00 50B2 | Reserved area (17 byte) | | | |
| 0x00 50B3 | RST | RST_SR | Reset status register | 0xFF ⁽¹⁾ |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 byte) | | | |
| 0x00 50C0 | CLK | CLK_ICKR | Internal clock control register | 0x01 |
| 0x00 50C1 | | CLK_ECKR | External clock control register | 0x00 |
| 0x00 50C2 | Reserved area (1 byte) | | | |
| 0x00 50C3 | CLK | CLK_CMSR | Clock master status register | 0xE1 |
| 0x00 50C4 | | CLK_SWR | Clock master switch register | 0xE1 |
| 0x00 50C5 | | CLK_SWCR | Clock switch control register | 0xFF |
| 0x00 50C6 | | CLK_CKDIVR | Clock divider register | 0x18 |
| 0x00 50C7 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0xFF |
| 0x00 50C8 | | CLK_CSSR | Clock security system register | 0x00 |
| 0x00 50C9 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50CA | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0xFF |
| 0x00 50CB | Reserved area (1 byte) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---------------------------|-------------------------|----------------|--|---------------------|
| 0x00 50CC | CLK | CLK_HSITRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CD | | CLK_SWIMCCR | SWIM clock control register | 0bXXXX XXX0 |
| 0x00 50CE to 0x00 50D0 | Reserved area (3 byte) | | | |
| 0x00 50D1 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D2 | | WWDG_WR | WWDR window register | 0x7F |
| 0x00 50D3 to 0x00 50DF | Reserved area (13 byte) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX ⁽²⁾ |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 byte) | | | |
| 0x00 50F0 | AWU | AWU_CSR1 | AWU control/status register 1 | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 to 0x00 50FF | Reserved area (13 byte) | | | |
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 |
| 0x00 5203 | | SPI_SR | SPI status register | 0x02 |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 |
| 0x00 5205 | | SPI_CRCPR | SPI CRC polynomial register | 0x07 |
| 0x00 5206 | | SPI_RXCR | SPI Rx CRC register | 0x00 |
| 0x00 5207 | | SPI_TXCR | SPI Tx CRC register | 0x00 |
| 0x00 5208 to 0x00 520F | Reserved area (8 byte) | | | |
| 0x00 5210 | I2C | I2C_CR1 | I2C control register 1 | 0x00 |
| 0x00 5211 | | I2C_CR2 | I2C control register 2 | 0x00 |
| 0x00 5212 | | I2C_FREQR | I2C frequency register | 0x00 |
| 0x00 5213 | | I2C_OARL | I2C own address register low | 0x00 |
| 0x00 5214 | | I2C_OARH | I2C own address register high | 0x00 |
| 0x00 5215 | | Reserved | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|------------------------|-------------------------|----------------|------------------------------------|--------------|
| 0x00 5216 | I2C | I2C_DR | I2C data register | 0x00 |
| 0x00 5217 | | I2C_SR1 | I2C status register 1 | 0x00 |
| 0x00 5218 | | I2C_SR2 | I2C status register 2 | 0x00 |
| 0x00 5219 | | I2C_SR3 | I2C status register 3 | 0x00 |
| 0x00 521A | | I2C_ITR | I2C interrupt control register | 0x00 |
| 0x00 521B | | I2C_CCRL | I2C clock control register low | 0x00 |
| 0x00 521C | | I2C_CCRH | I2C clock control register high | 0x00 |
| 0x00 521D | | I2C_TRISER | I2C TRISE register | 0x02 |
| 0x00 521E | | I2C_PECR | I2C packet error checking register | 0x00 |
| 0x00 521F to 0x00 522F | Reserved area (17 byte) | | | |
| 0x00 5230 | UART1 | UART1_SR | UART1 status register | 0xC0 |
| 0x00 5231 | | UART1_DR | UART1 data register | 0xFF |
| 0x00 5232 | | UART1_BRR1 | UART1 baud rate register 1 | 0x00 |
| 0x00 5233 | | UART1_BRR2 | UART1 baud rate register 2 | 0x00 |
| 0x00 5234 | | UART1_CR1 | UART1 control register 1 | 0x00 |
| 0x00 5235 | | UART1_CR2 | UART1 control register 2 | 0x00 |
| 0x00 5236 | | UART1_CR3 | UART1 control register 3 | 0x00 |
| 0x00 5237 | | UART1_CR4 | UART1 control register 4 | 0x00 |
| 0x00 5238 | | UART1_CR5 | UART1 control register 5 | 0x00 |
| 0x00 5239 | | UART1_GTR | UART1 guard time register | 0x00 |
| 0x00 523A | | UART1_PSCR | UART1 prescaler register | 0x00 |
| 0x00 523B to 0x00 523F | Reserved area (5 bytes) | | | |
| 0x00 523B to 0x00523F | Reserved area (21 byte) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|------------------------|--------------------------|---------------------------------|--|--------------|
| 0x00 5250 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 5251 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 5252 | | TIM1_SMCR | TIM1 slave mode control register | 0x00 |
| 0x00 5253 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 5254 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 5255 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 5256 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 5257 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 5258 | | TIM1_CCMR1 | TIM1 capture/compare mode register 1 | 0x00 |
| 0x00 5259 | | TIM1_CCMR2 | TIM1 capture/compare mode register 2 | 0x00 |
| 0x00 525A | | TIM1_CCMR3 | TIM1 capture/compare mode register 3 | 0x00 |
| 0x00 525B | | TIM1_CCMR4 | TIM1 capture/compare mode register 4 | 0x00 |
| 0x00 525C | | TIM1_CCER1 | TIM1 capture/compare enable register 1 | 0x00 |
| 0x00 525D | | TIM1_CCER2 | TIM1 capture/compare enable register 2 | 0x00 |
| 0x00 525E | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 525F | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 5260 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 5261 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 5262 | | TIM1_ARRH | TIM1 auto-reload register high | 0xFF |
| 0x00 5263 | | TIM1_ARRL | TIM1 auto-reload register low | 0xFF |
| 0x00 5264 | | TIM1_RCR | TIM1 repetition counter register | 0x00 |
| 0x00 5265 | | TIM1_CCR1H | TIM1 capture/compare register 1 high | 0x00 |
| 0x00 5266 | | TIM1_CCR1L | TIM1 capture/compare register 1 low | 0x00 |
| 0x00 5267 | | TIM1_CCR2H | TIM1 capture/compare register 2 high | 0x00 |
| 0x00 5268 | | TIM1_CCR2L | TIM1 capture/compare register 2 low | 0x00 |
| 0x00 5269 | | TIM1_CCR3H | TIM1 capture/compare register 3 high | 0x00 |
| 0x00 526A | | TIM1_CCR3L | TIM1 capture/compare register 3 low | 0x00 |
| 0x00 526B | | TIM1_CCR4H | TIM1 capture/compare register 4 high | 0x00 |
| 0x00 526C | | TIM1_CCR4L | TIM1 capture/compare register 4 low | 0x00 |
| 0x00 526D | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 526E | TIM1_DTR | TIM1 dead-time register | 0x00 | |
| 0x00 526F | TIM1_OISR | TIM1 output idle state register | 0x00 | |
| 0x00 5270 to 0x00 52FF | Reserved area (147 byte) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|------------------------|-------------------------|--------------------------------------|--|--------------|
| 0x00 5300 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5301 | | Reserved | | |
| 0x00 5302 | | Reserved | | |
| 0x00 5303 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5304 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5305 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5306 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5307 | | TIM2_CCMR1 | TIM2 capture/compare mode register 1 | 0x00 |
| 0x00 5308 | | TIM2_CCMR2 | TIM2 capture/compare mode register 2 | 0x00 |
| 0x00 5309 | | TIM2_CCMR3 | TIM2 capture/compare mode register 3 | 0x00 |
| 0x00 530A | | TIM2_CCER1 | TIM2 capture/compare enable register 1 | 0x00 |
| 0x00 530B | | TIM2_CCER2 | TIM2 capture/compare enable register 2 | 0x00 |
| 0x00 530C | | TIM2_CNTRH | TIM2 counter high | 0x00 |
| 0x00 530D | | TIM2_CNTRL | TIM2 counter low | 0x00 |
| 0x00 530E | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 530F | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 5310 | | TIM2_ARRL | TIM2 auto-reload register low | 0xFF |
| 0x00 5311 | | TIM2_CCR1H | TIM2 capture/compare register 1 high | 0x00 |
| 0x00 5312 | | TIM2_CCR1L | TIM2 capture/compare register 1 low | 0x00 |
| 0x00 5313 | | TIM2_CCR2H | TIM2 capture/compare reg. 2 high | 0x00 |
| 0x00 5314 | | TIM2_CCR2L | TIM2 capture/compare register 2 low | 0x00 |
| 0x00 5315 | TIM2_CCR3H | TIM2 capture/compare register 3 high | 0x00 | |
| 0x00 5316 | TIM2_CCR3L | TIM2 capture/compare register 3 low | 0x00 | |
| 0x00 5317 to 0x00 533F | Reserved area (43 byte) | | | |
| 0x00 5340 | TIM4 | TIM4_CR1 | TIM4 control register 1 | 0x00 |
| 0x00 5341 | | Reserved | | |
| 0x00 5342 | | Reserved | | |
| 0x00 5343 | | TIM4_IER | TIM4 interrupt enable register | 0x00 |
| 0x00 5344 | | TIM4_SR | TIM4 status register | 0x00 |
| 0x00 5345 | | TIM4_EGR | TIM4 event generation register | 0x00 |
| 0x00 5346 | | TIM4_CNTR | TIM4 counter | 0x00 |
| 0x00 5347 | | TIM4_PSCR | TIM4 prescaler register | 0x00 |
| 0x00 5348 | | TIM4_ARR | TIM4 auto-reload register | 0xFF |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---------------------------|---------------------------|----------------|---|--------------|
| 0x00 5349 to 0x00 53DF | Reserved area (153 byte) | | | |
| 0x00 53E0 to 0x00 53F3 | ADC1 | ADC_DBxR | ADC data buffer registers | 0x00 |
| 0x00 53F4 to 0x00 53FF | Reserved area (12 byte) | | | |
| 0x00 5400 | ADC1 | ADC_CSR | ADC control/status register | 0x00 |
| 0x00 5401 | | ADC_CR1 | ADC configuration register 1 | 0x00 |
| 0x00 5402 | | ADC_CR2 | ADC configuration register 2 | 0x00 |
| 0x00 5403 | | ADC_CR3 | ADC configuration register 3 | 0x00 |
| 0x00 5404 | | ADC_DRH | ADC data register high | 0xXX |
| 0x00 5405 | | ADC_DRL | ADC data register low | 0xXX |
| 0x00 5406 | | ADC_TDRH | ADC Schmitt trigger disable register high | 0x00 |
| 0x00 5407 | | ADC_TDRL | ADC Schmitt trigger disable register low | 0x00 |
| 0x00 5408 | | ADC_HTRH | ADC high threshold register high | 0x03 |
| 0x00 5409 | | ADC_HTRL | ADC high threshold register low | 0xFF |
| 0x00 540A | | ADC_LTRH | ADC low threshold register high | 0x00 |
| 0x00 540B | | ADC_LTRL | ADC low threshold register low | 0x00 |
| 0x00 540C | | ADC_AWSRH | ADC analog watchdog status register high | 0x00 |
| 0x00 540D | | ADC_AWSRL | ADC analog watchdog status register low | 0x00 |
| 0x00 540E | | ADC_AWCRH | ADC analog watchdog control register high | 0x00 |
| 0x00 540F | | ADC_AWCRL | ADC analog watchdog control register low | 0x00 |
| 0x00 5410 to 0x00 57FF | Reserved area (1008 byte) | | | |

1. Depends on the previous reset source.
2. Write only register.

6.2.3 CPU/SWIM/debug module/interrupt controller registers

Table 9. CPU/SWIM/debug module/interrupt controller registers

| Address | Block | Register Label | Register Name | Reset Status | |
|------------------------|-------------------------|-------------------------|--|-------------------------------|------|
| 0x00 7F00 | CPU ⁽¹⁾ | A | Accumulator | 0x00 | |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 | |
| 0x00 7F02 | | PCH | Program counter high | 0x00 | |
| 0x00 7F03 | | PCL | Program counter low | 0x00 | |
| 0x00 7F04 | | XH | X index register high | 0x00 | |
| 0x00 7F05 | | XL | X index register low | 0x00 | |
| 0x00 7F06 | | YH | Y index register high | 0x00 | |
| 0x00 7F07 | | YL | Y index register low | 0x00 | |
| 0x00 7F08 | | SPH | Stack pointer high | 0x | |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF | |
| 0x00 7F0A | | CCR | Condition code register | 0x28 | |
| 0x00 7F0B to 0x00 7F5F | | Reserved area (85 byte) | | | |
| 0x00 7F60 | | CPU | CFG_GCR | Global configuration register | 0x00 |
| 0x00 7F70 | ITC | ITC_SPR1 | Interrupt software priority register 1 | 0xFF | |
| 0x00 7F71 | | ITC_SPR2 | Interrupt software priority register 2 | 0xFF | |
| 0x00 7F72 | | ITC_SPR3 | Interrupt software priority register 3 | 0xFF | |
| 0x00 7F73 | | ITC_SPR4 | Interrupt software priority register 4 | 0xFF | |
| 0x00 7F74 | | ITC_SPR5 | Interrupt software priority register 5 | 0xFF | |
| 0x00 7F75 | | ITC_SPR6 | Interrupt software priority register 6 | 0xFF | |
| 0x00 7F76 | | ITC_SPR7 | Interrupt software priority register 7 | 0xFF | |
| 0x00 7F77 | | ITC_SPR8 | Interrupt software priority register 8 | 0xFF | |
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 byte) | | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 | |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 byte) | | | | |

Table 9. CPU/SWIM/debug module/interrupt controller registers (continued)

| Address | Block | Register Label | Register Name | Reset Status |
|---------------------------|-------|------------------------|---|--------------|
| 0x00 7F90 | DM | DM_BK1RE | DM breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | DM breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | DM breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | DM breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | DM breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | DM breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | DM debug module control register 1 | 0x00 |
| 0x00 7F97 | | DM_CR2 | DM debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | DM debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | DM debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | DM enable function register | 0xFF |
| 0x00 7F9B to 0x00 7F9F | | Reserved area (5 byte) | | |

1. Accessible by debug module only

7 Interrupt vector mapping

Table 10. Interrupt mapping

| IRQ no. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Vector address |
|----------|--------------|---|-----------------------|------------------------------|---------------------------|
| - | RESET | Reset | Yes | Yes | 0x00 8000 |
| - | TRAP | Software interrupt | - | - | 0x00 8004 |
| 0 | TLI | External top level interrupt | - | - | 0x00 8008 |
| 1 | AWU | Auto wake up from halt | - | Yes | 0x00 800C |
| 2 | CLK | Clock controller | - | - | 0x00 8010 |
| 3 | EXTI0 | Port A external interrupts | Yes ⁽¹⁾ | Yes ⁽¹⁾ | 0x00 8014 |
| 4 | EXTI1 | Port B external interrupts | Yes | Yes | 0x00 8018 |
| 5 | EXTI2 | Port C external interrupts | Yes | Yes | 0x00 801C |
| 6 | EXTI3 | Port D external interrupts | Yes | Yes | 0x00 8020 |
| 7 | EXTI4 | Port E external interrupts | Yes | Yes | 0x00 8024 |
| 8 | - | Reserved | | | 0x00 8028 |
| 9 | - | Reserved | | | 0x00 802C |
| 10 | SPI | End of transfer | Yes | Yes | 0x00 8030 |
| 11 | TIM1 | TIM1 update/overflow/underflow/ trigger/break | - | - | 0x00 8034 |
| 12 | TIM1 | TIM1 capture/compare | - | - | 0x00 8038 |
| 13 | TIM2 | TIM2 update /overflow | - | - | 0x00 803C |
| 14 | TIM2 | TIM2 capture/compare | - | - | 0x00 8040 |
| 15 | - | Reserved | | | 0x00 8044 |
| 16 | - | Reserved | | | 0x00 8048 |
| 17 | UART1 | Tx complete | - | - | 0x00 804C |
| 18 | UART1 | Receive register DATA FULL | - | - | 0x00 8050 |
| 19 | I2C | I2C interrupt | Yes | Yes | 0x00 8054 |
| 20 | - | Reserved | | | 0x00 8058 |
| 21 | - | Reserved | | | 0x00 805C |
| 22 | ADC1 | ADC1 end of conversion/analog watchdog interrupt | - | - | 0x00 8060 |
| 23 | TIM4 | TIM4 update/overflow | - | - | 0x00 8064 |
| 24 | Flash | EOP/WR_PG_DIS | - | - | 0x00 8068 |
| Reserved | | | | | 0x00 806C to 0x00 807C |

1. Except PA1

8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in [Table 11: Option bytes](#) below. Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option bytes

| Addr. | Option name | Option byte no. | Option bits | | | | | | | | Factory default setting |
|--------|------------------------------------|-----------------|--------------|-------|-------|-----------|----------|------------|----------|------------|-------------------------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0x00 |
| 0x4801 | User boot code (UBC) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 0x4802 | | NOPT1 | NUBC[7:0] | | | | | | | | 0xFF |
| 0x4803 | Alternate function remapping (AFR) | OPT2 | AFR7 | AFR6 | AFR5 | AFR4 | AFR3 | AFR2 | AFR1 | AFR0 | 0x00 |
| 0x4804 | | NOPT2 | NAFR7 | NAFR6 | NAFR5 | NAFR4 | NAFR3 | NAFR2 | NAFR1 | NAFR0 | 0xFF |
| 0x4805 | Misc. option | OPT3 | Reserved | | | HSITRIM | LSI_EN | IWDG_HW | WWDG_HW | WWDG_HALT | 0x00 |
| 0x4806 | | NOPT3 | Reserved | | | NHSI TRIM | NLSI_EN | NIWDG_HW | NWWDG_HW | NWWDG_HALT | 0xFF |
| 0x4807 | Clock option | OPT4 | Reserved | | | | EXT CLK | CKAWU SEL | PRS C1 | PRS C0 | 0x00 |
| 0x4808 | | NOPT4 | Reserved | | | | NEXT CLK | NCKAW USEL | NPR SC1 | NPR SC0 | 0xFF |
| 0x4809 | HSE clock startup | OPT5 | HSECNT[7:0] | | | | | | | | 0x00 |
| 0x480A | | NOPT5 | NHSECNT[7:0] | | | | | | | | 0xFF |

Table 12. Option byte description

| Option byte no. | Description |
|-----------------|--|
| OPT0 | <p>ROP[7:0] Memory readout protection (ROP)</p> <p>0xAA: Enable readout protection (write access via SWIM protocol)</p> <p>Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.</p> |

Table 12. Option byte description (continued)

| Option byte no. | Description |
|-----------------|--|
| OPT1 | <p>UBC[7:0] <i>User boot code area</i> 0x00: no UBC, no write-protection 0x01: Pages 0 defined as UBC, memory write-protected 0x02: Pages 0 to 1 defined as UBC, memory write-protected Page 0 and page 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory-write protected. <i>Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM write protection for more details.</i></p> |
| OPT2 | <p>AFR[7:0] Refer to the following section for alternate function remapping descriptions of bits [7:2] and [1:0] respectively.</p> |
| OPT3 | <p>HSITRIM: <i>high-speed internal clock trimming register size</i> 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register</p> <p>LSI_EN: <i>Low speed internal clock enable</i> 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source</p> <p>IWDG_HW: <i>Independent watchdog</i> 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware</p> <p>WWDG_HW: <i>Window watchdog activation</i> 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware</p> <p>WWDG_HALT: <i>Window watchdog reset on halt</i> 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active</p> |
| OPT4 | <p>EXTCLK: <i>External clock selection</i> 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN</p> <p>CKAWUSEL: <i>Auto wakeup unit/clock</i> 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU</p> <p>PRSC[1:0] <i>AWU clock prescaler</i> 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler</p> |
| OPT5 | <p>HSECNT[7:0]: <i>HSE crystal oscillator stabilization time</i> This configures the stabilization time. 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles</p> |

8.1 Alternate function remapping bits

Table 13. STM8S001J3 alternate function remapping bits for 8-pin devices

| Option byte number | Description |
|--------------------|---|
| OPT2 | AFR7 <i>Alternate function remapping option 7</i> 0: AFR7 remapping option inactive: default alternate function ⁽¹⁾ 1: Port C3 alternate function = TIM1_CH1N; port C4 alternate function = TIM1_CH2N. |
| | AFR6 <i>Alternate function remapping option 6</i> Reserved. |
| | AFR5 <i>Alternate function remapping option 5</i> Reserved. |
| | AFR4 <i>Alternate function remapping option 4</i> 0: AFR4 remapping option inactive: default alternate function ⁽¹⁾ . 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN. |
| | AFR3 <i>Alternate function remapping option 3</i> 0: AFR3 remapping option inactive: default alternate function ⁽¹⁾ 1: Port C3 alternate function = TLI. |
| | AFR2 <i>Alternate function remapping option 2</i> 0: AFR2 remapping option inactive: default alternate function ⁽¹⁾ 1: Port C4 alternate function = AIN2. |
| | AFR1 <i>Alternate function remapping option 1</i> ⁽²⁾ 0: AFR1 remapping option inactive: default alternate function ⁽¹⁾ 1: If AFR0=0: Port A3 alternate function = SPI_NSS If AFR0=1: Port A3 alternate function = UART_TX. |
| | AFR0 <i>Alternate function remapping option 0</i> ⁽²⁾ 0: AFR0 remapping option inactive: Default alternate functions ⁽¹⁾ 1: Port C5 alternate function = TIM2_CH1; port C6 alternate function = TIM1_CH1. |

1. Refer to the pinout description.

2. Do not use more than one remapping option in the same port.

9 Electrical characteristics

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

9.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = 5\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

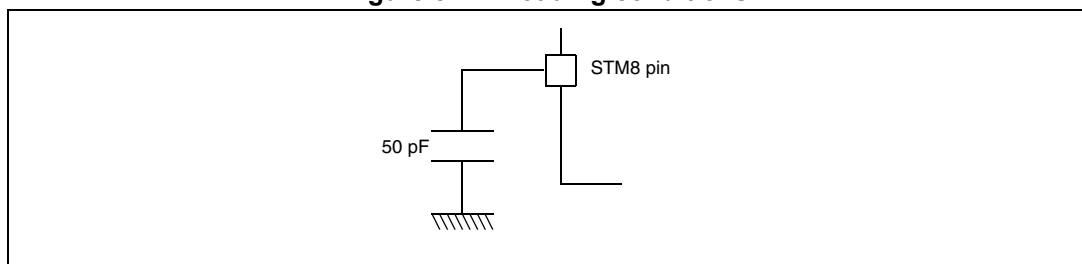
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 5](#).

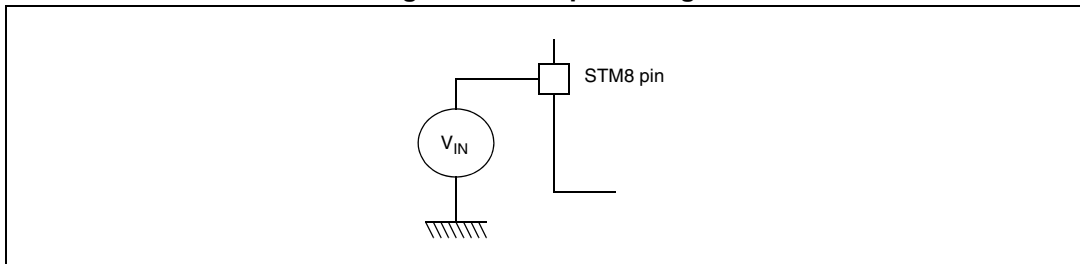
Figure 5. Pin loading conditions



9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 6](#).

Figure 6. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 14: Voltage characteristics](#), [Table 15: Current characteristics](#), and [Table 16: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 14. Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|--------------------|--|--|----------------|------|
| $V_{DDx} - V_{SS}$ | Supply voltage ⁽¹⁾ | -0.3 | 6.5 | V |
| V_{IN} | Input voltage on true open drain pins ⁽²⁾ | $V_{SS} - 0.3$ | 6.5 | |
| | Input voltage on any other pin ⁽²⁾ | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | |
| V_{ESD} | Electrostatic discharge voltage | see Absolute maximum ratings (electrical sensitivity) on page 74 | | - |

- All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
- $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 15. Current characteristics

| Symbol | Ratings | Max. ⁽¹⁾ | Unit |
|--------------------------------------|---|---------------------|------|
| I_{VDD} | Total current into V_{DD} power lines (source) ⁽²⁾ | 100 | mA |
| I_{VSS} | Total current out of V_{SS} ground lines (sink) ⁽²⁾ | 80 | |
| I_{IO} | Output current sunk by any I/O and control pin | 20 | |
| | Output current source by any I/Os and control pin | -20 | |
| $I_{INJ(PIN)}$ ⁽³⁾⁽⁴⁾ | Injected current on OSCIN pin | ±4 | |
| | Injected current on any other pin ⁽⁵⁾ | ±4 | |
| $\Sigma I_{INJ(PIN)}$ ⁽³⁾ | Total injected current (sum of all I/O and control pins) ⁽⁵⁾ | ±20 | |

1. Guaranteed by characterization results.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 16. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|-----------|------------------------------|------------|------|
| T_{STG} | Storage temperature range | -65 to 150 | °C |
| T_J | Maximum junction temperature | 150 | |

9.3 Operating conditions

The device must be used in operating conditions that respect the parameters in [Table 17](#). In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 17. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|---|---------------------------|------|------|------|
| f_{CPU} | Internal CPU clock frequency | - | 0 | 16 | MHz |
| V_{DD} | Standard operating voltage | - | 2.95 | 5.5 | V |
| $V_{CAP}^{(1)}$ | C_{EXT} : capacitance of external capacitor | - | 470 | 3300 | nF |
| | ESR of external capacitor | At 1 MHz ⁽²⁾ | - | 0.3 | ohm |
| | ESL of external capacitor | | - | 15 | nH |
| $P_D^{(3)}$ | Power dissipation at $T_A = 125^\circ C$ | SO8N | - | 49 | mW |
| T_A | Ambient temperature | Maximum power dissipation | -40 | 125 | °C |
| T_J | Junction temperature range | - | -40 | 130 | |

- Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter must be respected for the full application range.
- This frequency of 1 MHz as a condition for V_{CAP} parameters is given by the design of the internal regulator.
- To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A) / \Theta_{JA}$ (see [Section 10.2: Thermal characteristics on page 78](#)) with the value for T_{Jmax} given in [Table 17](#) above and the value for Θ_{JA} given in [Table 49: Thermal characteristics](#).

Figure 7. f_{CPUmax} versus V_{DD}

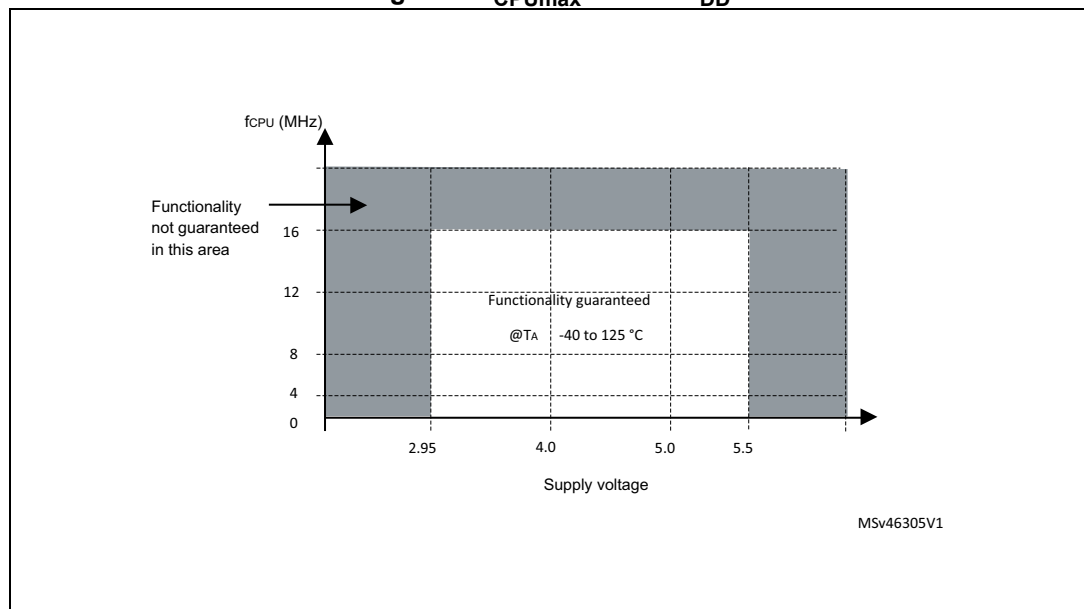


Table 18. Operating conditions at power-up/power-down

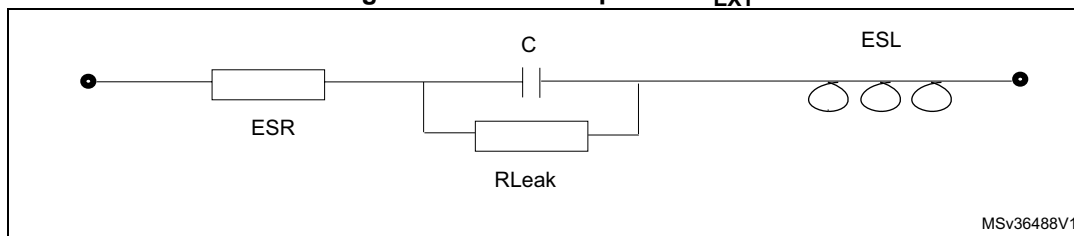
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|-----------------|-----|------|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | - | 2 | - | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate ⁽¹⁾ | - | 2 | - | ∞ | |
| t_{TEMP} | Reset release delay | V_{DD} rising | - | - | 1.7 | ms |
| V_{IT+} | Power-on reset threshold | - | 2.6 | 2.7 | 2.85 | V |
| V_{IT-} | Brown-out reset threshold | - | 2.5 | 2.65 | 2.8 | V |
| $V_{HYS(BOR)}$ | Brown-out reset hysteresis | - | - | 70 | - | mV |

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage ($V_{DD \text{ min}}$) when the t_{TEMP} delay has elapsed.

9.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in [Table 17](#). Care should be taken to limit the series inductance to less than 15 nH.

Figure 8. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

9.3.2 Supply current characteristics

The current consumption is measured as described in [Section 9.1.5: Pin input voltage](#).

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by Peripheral Clock Gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A .

Table 19. Total current consumption with code execution in run mode at $V_{DD} = 5 V$

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|---|--|--|---------------------------------------|------|--------------------|------|
| $I_{DD(RUN)}$ | Supply current in run mode, code executed from RAM | $f_{CPU} = f_{MASTER} = 16 \text{ MHz}$ | HSE user ext. clock (16 MHz) | 2 | 2.35 | mA |
| | | | HSI RC osc. (16 MHz) | 1.7 | 2 | |
| | | $f_{CPU} = f_{MASTER}/128 = 125 \text{ kHz}$ | HSE user ext. clock (16 MHz) | 0.86 | - | |
| | | | HSI RC osc. (16 MHz) | 0.7 | 0.87 | |
| | $f_{CPU} = f_{MASTER}/128 = 15.625 \text{ kHz}$ | HSI RC osc. (16 MHz/8) | 0.46 | 0.58 | | |
| | $f_{CPU} = f_{MASTER} = 128 \text{ kHz}$ | LSI RC osc. (128 kHz) | 0.41 | 0.55 | | |
| | Supply current in run mode, code executed from Flash | $f_{CPU} = f_{MASTER} = 16 \text{ MHz}$ | HSE user ext. clock (16 MHz) | 4.3 | 4.75 | |
| | | | HSI RC osc. (16 MHz) | 3.7 | 4.5 | |
| | | $f_{CPU} = f_{MASTER} = 2 \text{ MHz}$ | HSI RC osc. (16 MHz/8) ⁽²⁾ | 0.84 | 1.05 | |
| | | $f_{CPU} = f_{MASTER}/128 = 125 \text{ kHz}$ | HSI RC osc. (16 MHz) | 0.72 | 0.9 | |
| $f_{CPU} = f_{MASTER}/128 = 15.625 \text{ kHz}$ | | HSI RC osc. (16 MHz/8) | 0.46 | 0.58 | | |
| $f_{CPU} = f_{MASTER} = 128 \text{ kHz}$ | | LSI RC osc. (128 kHz) | 0.42 | 0.57 | | |

1. Guaranteed by characterization results.

2. Default clock configuration measured with all peripherals off.

Table 20. Total current consumption with code execution in run mode at $V_{DD} = 3.3\text{ V}$

| Symbol | Parameter | Conditions | Typ | Max ⁽¹⁾ | Unit | |
|---------------|--|--|---------------------------------------|--------------------|------|----|
| $I_{DD(RUN)}$ | Supply current in run mode, code executed from RAM | $f_{CPU} = f_{MASTER} = 16\text{ MHz}$ | HSE user ext. clock (16 MHz) | 2 | 2.3 | mA |
| | | | HSI RC osc. (16 MHz) | 1.5 | 2 | |
| | | $f_{CPU} = f_{MASTER}/128 = 125\text{ kHz}$ | HSE user ext. clock (16 MHz) | 0.81 | - | |
| | | | HSI RC osc. (16 MHz) | 0.7 | 0.87 | |
| | | $f_{CPU} = f_{MASTER}/128 = 15.625\text{ kHz}$ | HSI RC osc. (16MHz/8) | 0.46 | 0.58 | |
| | | $f_{CPU} = f_{MASTER} = 128\text{ kHz}$ | LSI RC osc. (128 kHz) | 0.41 | 0.55 | |
| | Supply current in run mode, code executed from Flash | $f_{CPU} = f_{MASTER} = 16\text{ MHz}$ | HSE user ext. clock (16 MHz) | 3.9 | 4.7 | |
| | | | HSI RC osc. (16 MHz) | 3.7 | 4.5 | |
| | | $f_{CPU} = f_{MASTER} = 2\text{ MHz}$ | HSI RC osc. (16 MHz/8) ⁽²⁾ | 0.84 | 1.05 | |
| | | $f_{CPU} = f_{MASTER}/128 = 125\text{ kHz}$ | HSI RC osc. (16 MHz) | 0.72 | 0.9 | |
| | | $f_{CPU} = f_{MASTER}/128 = 15.625\text{ kHz}$ | HSI RC osc. (16 MHz/8) | 0.46 | 0.58 | |
| | | $f_{CPU} = f_{MASTER} = 128\text{ kHz}$ | LSI RC osc. (128 kHz) | 0.42 | 0.57 | |

1. Guaranteed by characterization results.

2. Default clock configuration, measured with all peripherals off.

Total current consumption in wait mode

Table 21. Total current consumption in wait mode at V_{DD} = 5 V

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|----------------------|-----------------------------|--|---------------------------------------|------|--------------------|------|
| I _{DD(WFI)} | Supply current in wait mode | f _{CPU} = f _{MASTER} = 16 MHz | HSE user ext. clock (16 MHz) | 1.1 | 1.3 | mA |
| | | | HSI RC osc. (16 MHz) | 0.89 | 1.1 | |
| | | f _{CPU} = f _{MASTER} /128 = 125 kHz | HSI RC osc. (16 MHz) | 0.7 | 0.88 | |
| | | f _{CPU} = f _{MASTER} /128 = 15.625 kHz | HSI RC osc. (16 MHz/8) ⁽²⁾ | 0.45 | 0.57 | |
| | | f _{CPU} = f _{MASTER} = 128 kHz | LSI RC osc. (128 kHz) | 0.4 | 0.54 | |

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Table 22. Total current consumption in wait mode at V_{DD} = 3.3 V

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|----------------------|-----------------------------|--|---------------------------------------|------|--------------------|------|
| I _{DD(WFI)} | Supply current in wait mode | f _{CPU} = f _{MASTER} = 16 MHz | HSE user ext. clock (16 MHz) | 1.1 | 1.3 | mA |
| | | | HSI RC osc. (16 MHz) | 0.89 | 1.1 | |
| | | f _{CPU} = f _{MASTER} /128 = 125 kHz | HSI RC osc. (16 MHz) | 0.7 | 0.88 | |
| | | f _{CPU} = f _{MASTER} /128 = 15.625 kHz | HSI RC osc. (16 MHz/8) ⁽²⁾ | 0.45 | 0.57 | |
| | | f _{CPU} = f _{MASTER} /128 = 15.625 kHz | LSI RC osc. (128 kHz) | 0.4 | 0.54 | |

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 23. Total current consumption in active halt mode at V_{DD} = 5 V

| Symbol | Parameter | Conditions | | | Typ | Max at 85°C ⁽¹⁾ | Max at 125°C ⁽¹⁾ | Unit |
|---------------------|------------------------------------|---|---------------------------|----------------------------------|------|----------------------------|-----------------------------|------|
| | | Main voltage regulator (MVR) ⁽²⁾ | Flash mode ⁽³⁾ | Clock source | | | | |
| I _{DD(AH)} | Supply current in active halt mode | On | Operating mode | HSE user external clock (16 MHz) | 1030 | - | - | µA |
| | | | | LSI RC oscillator (128 kHz) | 200 | 260 | 300 | |
| | | | Power-down mode | HSE user external clock (16 MHz) | 970 | - | - | |
| | | | | LSI RC oscillator (128 kHz) | 150 | 200 | 230 | |
| | | Off | Operating mode | LSI RC oscillator (128 kHz) | 66 | 85 | 110 | |
| | | | Power-down mode | | 10 | 20 | 40 | |

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 24. Total current consumption in active halt mode at V_{DD} = 3.3 V

| Symbol | Parameter | Conditions | | | Typ | Max at 85°C ⁽¹⁾ | Max at 125°C ⁽¹⁾ | Unit |
|---------------------|------------------------------------|---|---------------------------|----------------------------------|-----|----------------------------|-----------------------------|------|
| | | Main voltage regulator (MVR) ⁽²⁾ | Flash mode ⁽³⁾ | Clock source | | | | |
| I _{DD(AH)} | Supply current in active halt mode | On | Operating mode | HSE user external clock (16 MHz) | 550 | - | - | µA |
| | | | | LSI RC osc. (128 kHz) | 200 | 260 | 290 | |
| | | | Power-down mode | HSE user external clock (16 MHz) | 970 | - | - | |
| | | | | LSI RC osc. (128 kHz) | 150 | 200 | 230 | |
| | | Off | Operating mode | LSI RC osc. (128 kHz) | 66 | 80 | 105 | |
| | | | Power-down mode | | 10 | 18 | 35 | |

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

Table 25. Total current consumption in halt mode at V_{DD} = 5 V

| Symbol | Parameter | Conditions | Typ | Max at 85°C ⁽¹⁾ | Max at 125°C ⁽¹⁾ | Unit |
|--------------------|-----------------------------|--|-----|----------------------------|-----------------------------|------|
| I _{DD(H)} | Supply current in halt mode | Flash in operating mode, HSI clock after wakeup | 63 | 75 | 105 | μA |
| | | Flash in power-down mode, HSI clock after wakeup | 6.0 | 20 | 55 | |

1. Guaranteed by characterization results.

Table 26. Total current consumption in halt mode at V_{DD} = 3.3 V

| Symbol | Parameter | Conditions | Typ | Max at 85°C ⁽¹⁾ | Max at 125°C ⁽¹⁾ | Unit |
|--------------------|-----------------------------|--|-----|----------------------------|-----------------------------|------|
| I _{DD(H)} | Supply current in halt mode | Flash in operating mode, HSI clock after wakeup | 60 | 75 | 100 | μA |
| | | Flash in power-down mode, HSI clock after wakeup | 4.5 | 17 | 30 | |

1. Guaranteed by characterization results.

Low-power mode wakeup times

Table 27. Wakeup times

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit | |
|----------------------|--|--|---|--------------------|--------------------|------------------|----|
| t _{WU(WFI)} | Wakeup time from wait mode to run mode ⁽³⁾ | 0 to 16 MHz | | - | -(2) | | |
| | | f _{CPU} = f _{MASTER} = 16 MHz. | | 0.56 | - | | |
| t _{WU(AH)} | Wakeup time active halt mode to run mode. ⁽³⁾ | MVR voltage regulator on ⁽⁴⁾ | Flash in operating mode ⁽⁵⁾ | HSI (after wakeup) | 1 ⁽⁶⁾ | 2 ⁽⁶⁾ | μs |
| | | | Flash in power-down mode ⁽⁵⁾ | | 3 ⁽⁶⁾ | - | |
| | | MVR voltage regulator off ⁽⁴⁾ | Flash in operating mode ⁽⁵⁾ | | 48 ⁽⁶⁾ | - | |
| | | | Flash in power-down mode ⁽⁵⁾ | | 50 ⁽⁶⁾ | - | |
| t _{WU(H)} | Wakeup time from halt mode to run mode ⁽³⁾ | Flash in operating mode ⁽⁵⁾ | | 52 | - | | |
| | | Flash in power-down mode ⁽⁵⁾ | | 54 | - | | |

1. Guaranteed by design.
2. t_{WU(WFI)} = 2 × 1/f_{master} + 7 × 1/f_{CPU}
3. Measured from interrupt event to interrupt vector fetch.
4. Configured by the REGAH bit in the CLK_ICR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.



Total current consumption and timing in forced reset state

Table 28. Total current consumption and timing in forced reset state

| Symbol | Parameter | Conditions | Typ | Max ⁽¹⁾ | Unit |
|----------------------|--|-------------------------|-----|--------------------|------|
| I _{DD(R)} | Supply current in reset state ⁽²⁾ | V _{DD} = 5 V | 400 | - | μA |
| | | V _{DD} = 3.3 V | 300 | - | |
| t _{RESETBL} | Reset release to vector fetch | - | - | 150 | μs |

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, V_{DD} = 5 V.

Table 29. Peripheral current consumption

| Symbol | Parameter | Typ. | Unit |
|------------------------|--|------|------|
| I _{DD(TIM1)} | TIM1 supply current ⁽¹⁾ | 210 | μA |
| I _{DD(TIM2)} | TIM2 supply current ⁽¹⁾ | 130 | |
| I _{DD(TIM4)} | TIM4 timer supply current ⁽¹⁾ | 50 | |
| I _{DD(UART1)} | UART1 supply current ⁽¹⁾ | 120 | |
| I _{DD(SPI)} | SPI supply current ⁽¹⁾ | 45 | |
| I _{DD(I2C)} | I2C supply current ⁽¹⁾ | 65 | |
| I _{DD(ADC1)} | ADC1 supply current when converting ⁽¹⁾ | 1000 | |

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.

Current consumption curves

The following figures show the typical current consumption measured with code executing in RAM.

Figure 9. Typ. $I_{DD(RUN)}$ vs V_{DD} , HSE user external clock, $f_{CPU} = 16$ MHz

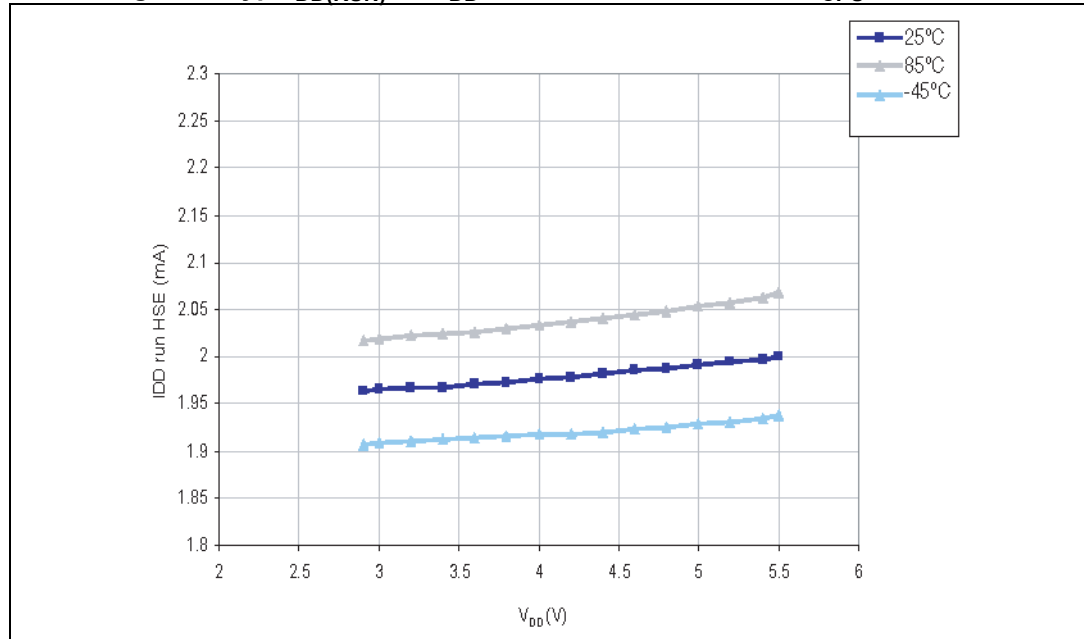


Figure 10. Typ. $I_{DD(RUN)}$ vs f_{CPU} , HSE user external clock, $V_{DD} = 5$ V

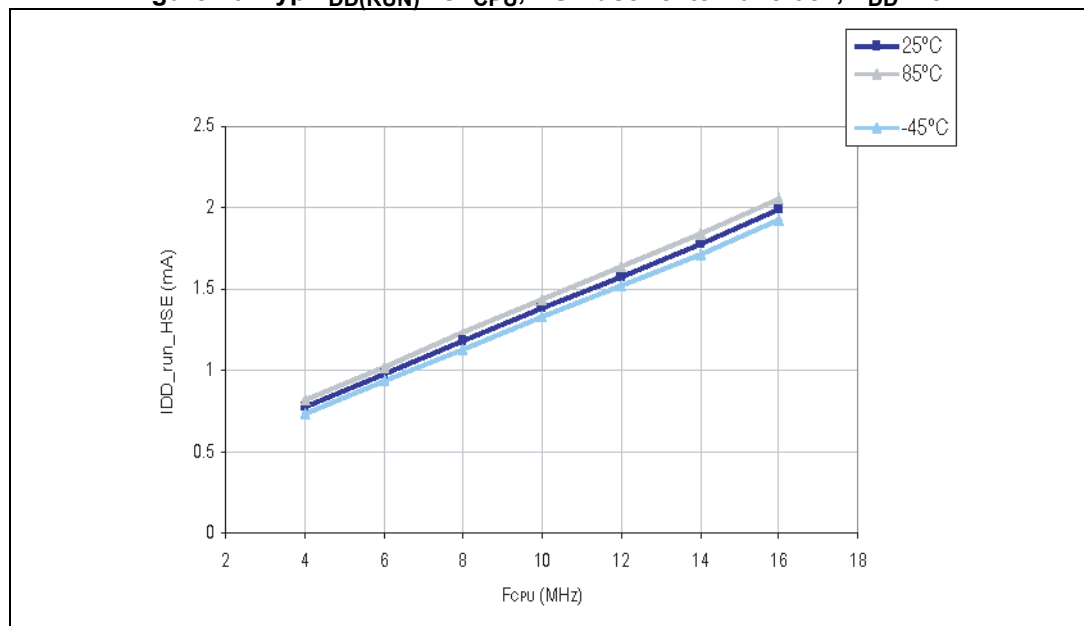


Figure 11. Typ. $I_{DD(RUN)}$ vs V_{DD} , HSI RC osc, $f_{CPU} = 16$ MHz

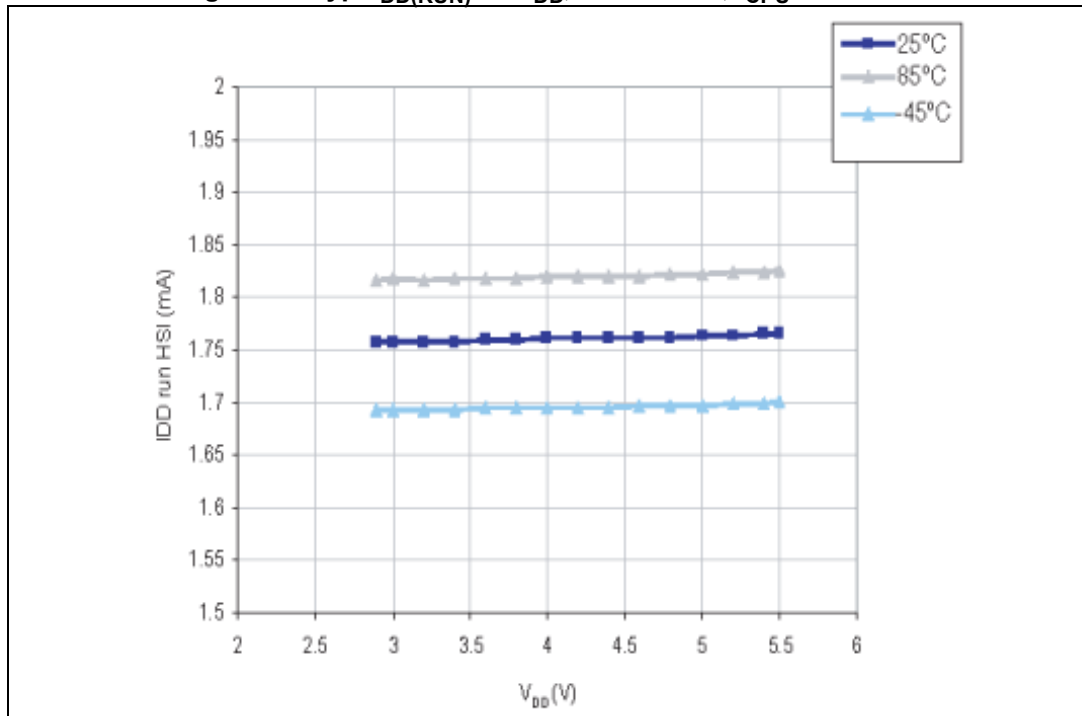


Figure 12. Typ. $I_{DD(WFI)}$ vs V_{DD} HSE user external clock, $f_{CPU} = 16$ MHz

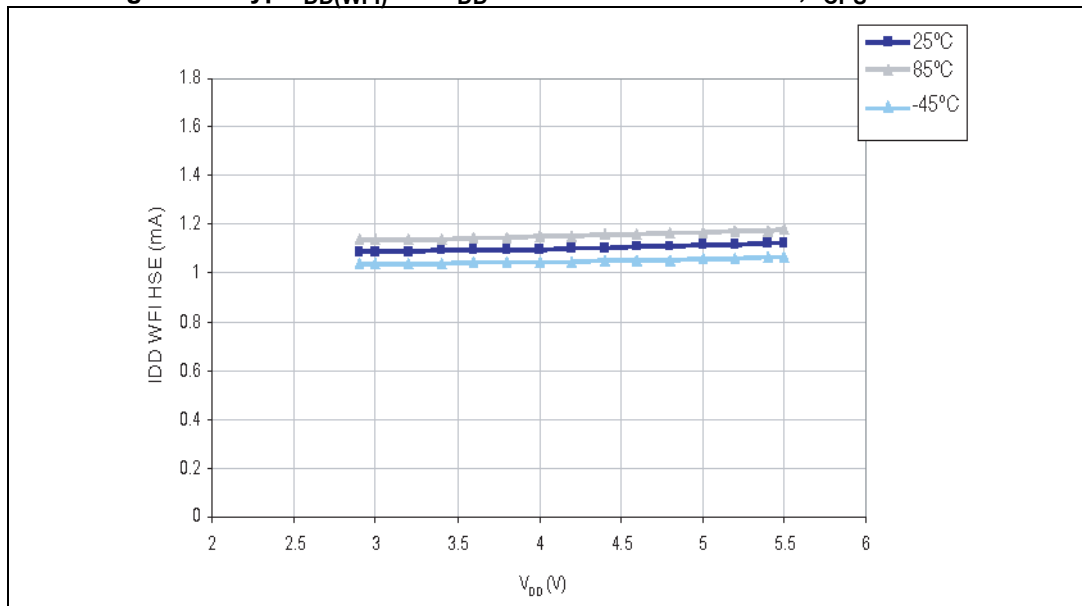


Figure 13. Typ. $I_{DD(WFI)}$ vs. f_{CPU} , HSE user external clock, $V_{DD} = 5\text{ V}$

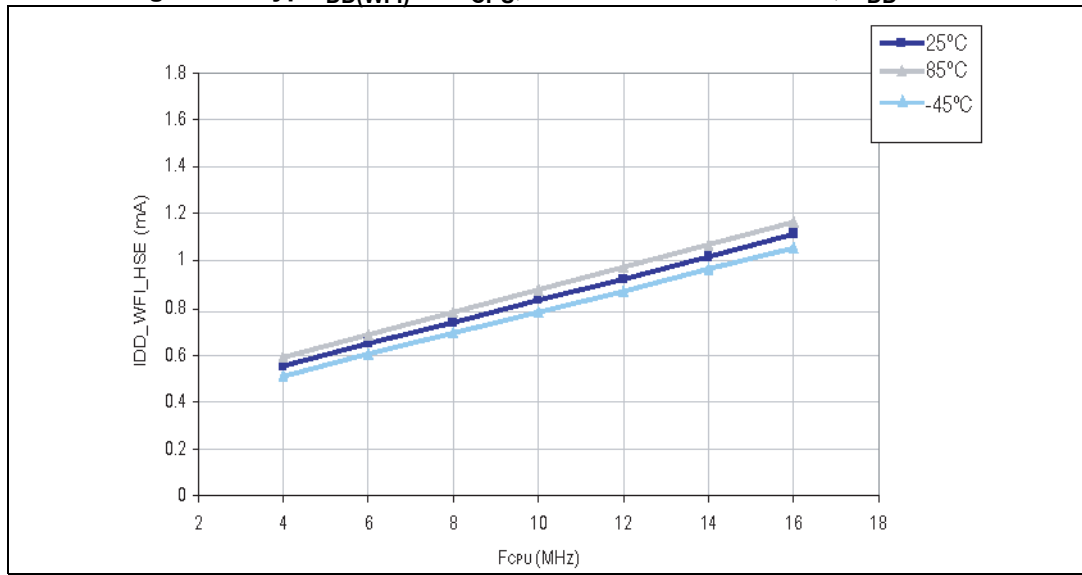
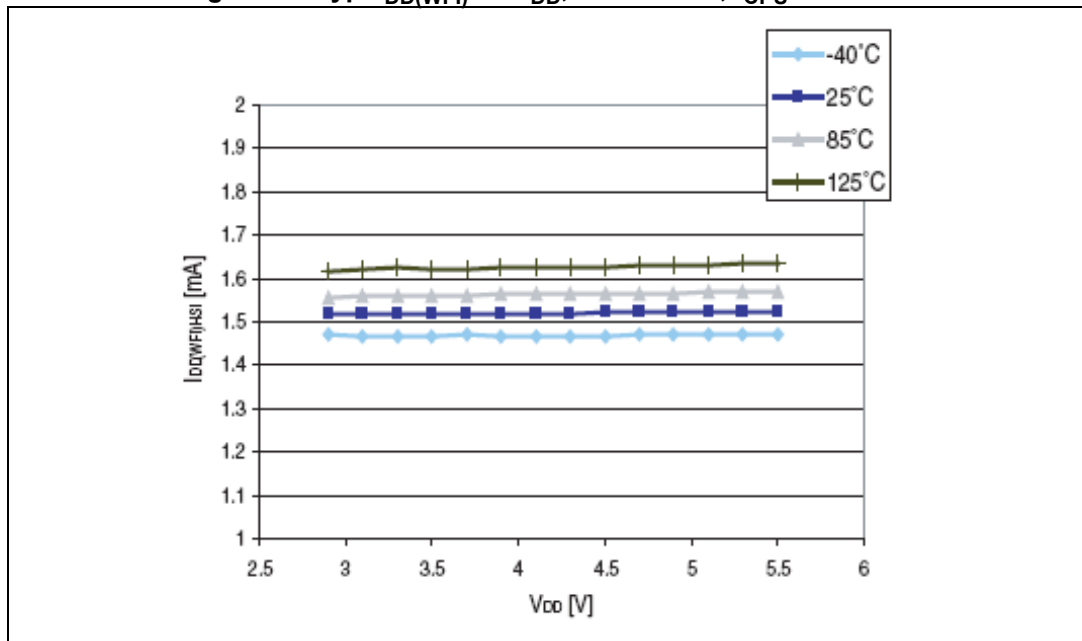


Figure 14. Typ. $I_{DD(WFI)}$ vs V_{DD} , HSI RC osc, $f_{CPU} = 16\text{ MHz}$



9.3.3 External clock sources and timing characteristics

HSE user external clock

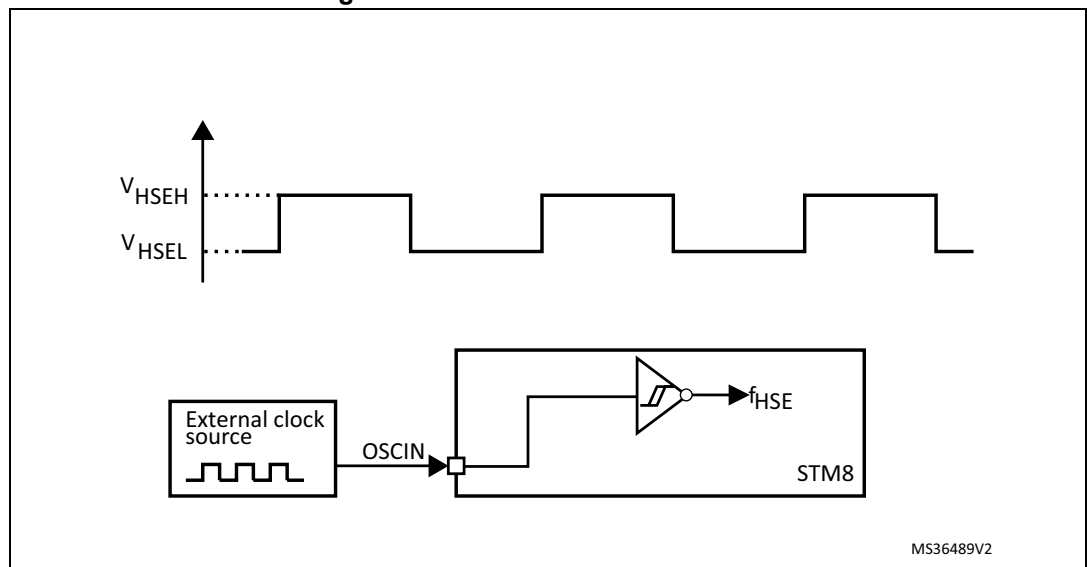
Subject to general operating conditions for V_{DD} and T_A .

Table 30. HSE user external clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------------------------|----------------------------|---------------------|-----|---------------------|---------|
| f_{HSE_ext} | User external clock source frequency | | 0 | - | 16 | MHz |
| $V_{HSEH}^{(1)}$ | OSCIN input pin high level voltage | - | $0.7 \times V_{DD}$ | - | $V_{DD} + 0.3 V$ | V |
| $V_{HSEL}^{(1)}$ | OSCIN input pin low level voltage | | V_{SS} | - | $0.3 \times V_{DD}$ | |
| I_{LEAK_HSE} | OSCIN input leakage current | $V_{SS} < V_{IN} < V_{DD}$ | -1 | - | +1 | μA |

1. Guaranteed by characterization results.

Figure 15. HSE external clock source



9.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A .

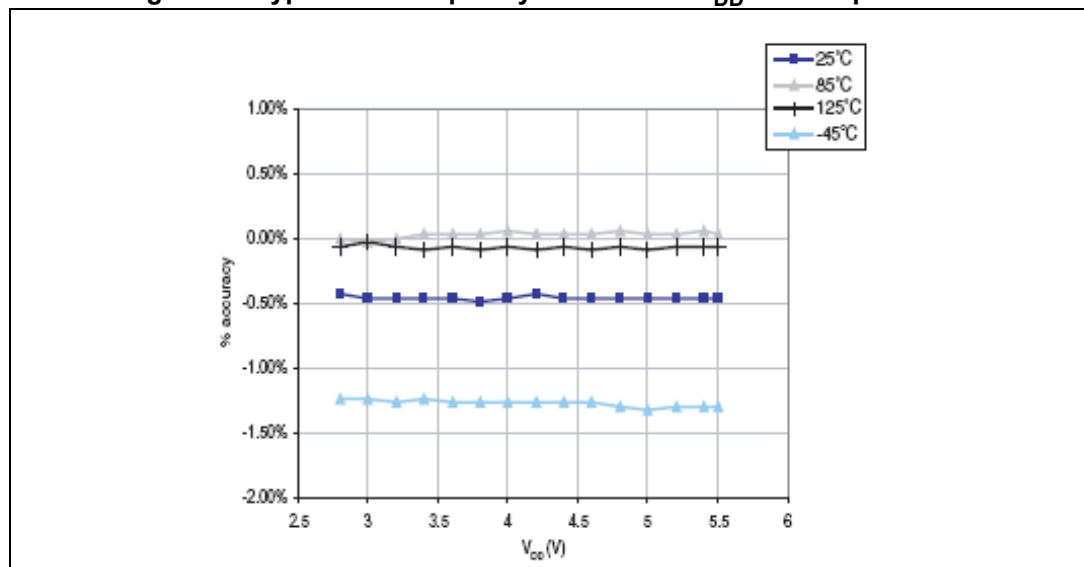
High speed internal RC oscillator (HSI)

Table 31. HSI oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|--|---|------------|--------|--------------------|---------------|
| f_{HSI} | Frequency | - | - | 16 | - | MHz |
| ACC_{HSI} | Accuracy of HSI oscillator | User-trimmed with the CLK_HSITRIMR register for given V_{DD} and T_A conditions ⁽¹⁾ | - | - | 1.0 ⁽²⁾ | % |
| | Accuracy of HSI oscillator (factory calibrated) | $V_{DD} = 5\text{ V}, T_A = 25\text{ }^\circ\text{C}$ $V_{DD} = 5\text{ V}, -40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ | -2.5 -5 | - - | 1.5 5 | |
| $t_{su(HSI)}$ | HSI oscillator wakeup time including calibration | - | - | - | 1.0 ⁽²⁾ | μs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | - | - | 170 | 250 ⁽³⁾ | μA |

1. See the application note.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Figure 16. Typical HSI frequency variation vs V_{DD} at 4 temperatures



Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A .

Table 32. LSI oscillator characteristics

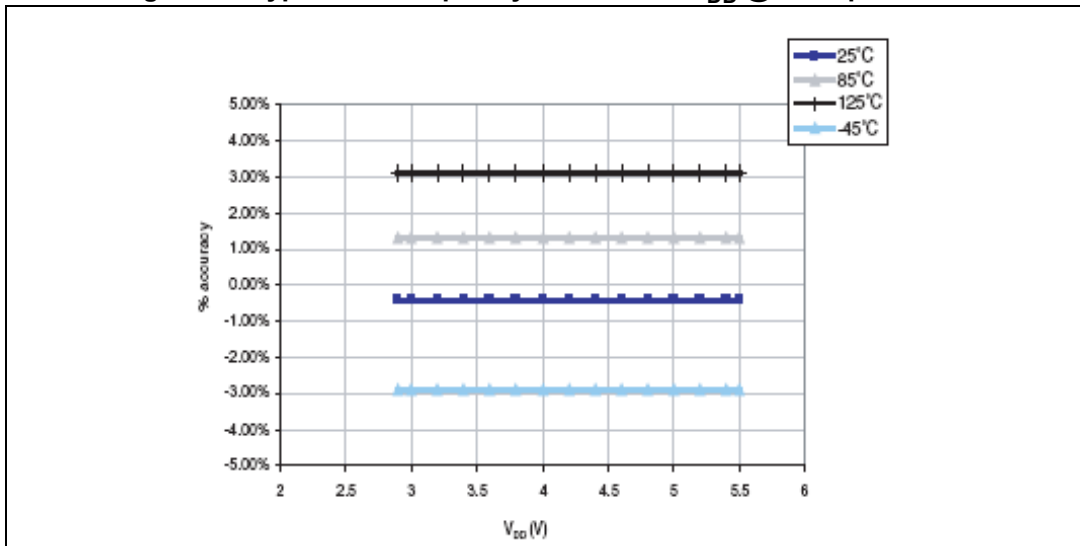
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-----------|------------|-----|-----|-----|------|
| f_{LSI} | Frequency | - | - | 128 | - | kHz |

Table 32. LSI oscillator characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------------------|------------|-----|-----|------------------|---------|
| $t_{su(LSI)}$ | LSI oscillator wakeup time | - | - | - | 7 ⁽¹⁾ | μs |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | - | - | 5 | - | μA |

1. Guaranteed by design.

Figure 17. Typical LSI frequency variation vs V_{DD} @ 4 temperatures



9.3.5 Memory characteristics

RAM and hardware registers

Table 33. RAM and hardware registers

| Symbol | Parameter | Conditions | Min | Unit |
|-----------------|------------------------------------|----------------------|------------------------------------|------|
| V _{RM} | Data retention mode ⁽¹⁾ | Halt mode (or reset) | V _{IT-max} ⁽²⁾ | V |

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design.

2. Refer to [Table 18 on page 43](#) for the value of V_{IT-max}.

Flash program memory and data EEPROM

General conditions: T_A = -40 to 85 °C.

Table 34. Flash program memory and data EEPROM

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max | Unit |
|--------------------|---|---------------------------|--------------------|-----|-----|--------|
| V _{DD} | Operating voltage (all modes, execution/write/erase) | f _{CPU} ≤ 16 MHz | 2.95 | - | 5.5 | V |
| t _{prog} | Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/64 bytes) | - | - | 6.0 | 6.6 | ms |
| | Fast programming time for 1 block (64 bytes) | - | - | 3.0 | 3.3 | ms |
| t _{erase} | Erase time for 1 block (64 bytes) | - | - | 3.0 | 3.3 | ms |
| N _{RW} | Erase/write cycles ⁽²⁾ (program memory) | T _A = 85 °C | 100 | - | - | cycles |
| | Erase/write cycles ⁽²⁾ (data memory) | | 100 k | - | - | |
| t _{RET} | Data retention (program memory) after 100 erase/write cycles at T _A = 85 °C | T _{RET} = 55° C | 20 | - | - | years |
| | Data retention (data memory) after 10 k erase/write cycles at T _A = 85 °C | | 20 | - | - | |
| | Data retention (data memory) after 100 k erase/write cycles at T _A = 125 °C | T _{RET} = 85° C | 1.0 | - | - | |
| I _{DD} | Supply current (Flash programming or erasing for 1 to 128 bytes) | - | - | 2.0 | - | mA |

1. Guaranteed by characterization results.

2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 35. I/O static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---|---|---------------------|-----|--------------------------|---------------|
| V_{IL} | Input low level voltage | $V_{DD} = 5\text{ V}$ | -0.3 | - | $0.3 \times V_{DD}$ | V |
| V_{IH} | Input high level voltage | | $0.7 \times V_{DD}$ | - | $V_{DD} + 0.3\text{ V}$ | V |
| V_{hys} | Hysteresis ⁽¹⁾ | | - | 700 | - | mV |
| R_{pu} | Pull-up resistor | $V_{DD} = 5\text{ V}, V_{IN} = V_{SS}$ | 30 | 55 | 80 | k Ω |
| t_R, t_F | Rise and fall time (10% - 90%) | Fast I/Os Load = 50 pF | - | - | 20 ⁽²⁾ | ns |
| | | Standard and high sink I/Os Load = 50 pF | - | - | 125 ⁽²⁾ | ns |
| I_{lkg} | Input leakage current, analog and digital | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ± 1 | μA |
| $I_{lkg\text{ ana}}$ | Analog input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ± 250 ⁽³⁾ | nA |
| $I_{lkg(inj)}$ | Leakage current in adjacent I/O | Injection current $\pm 4\text{ mA}$ | - | - | ± 1 ⁽³⁾ | μA |

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Figure 18. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

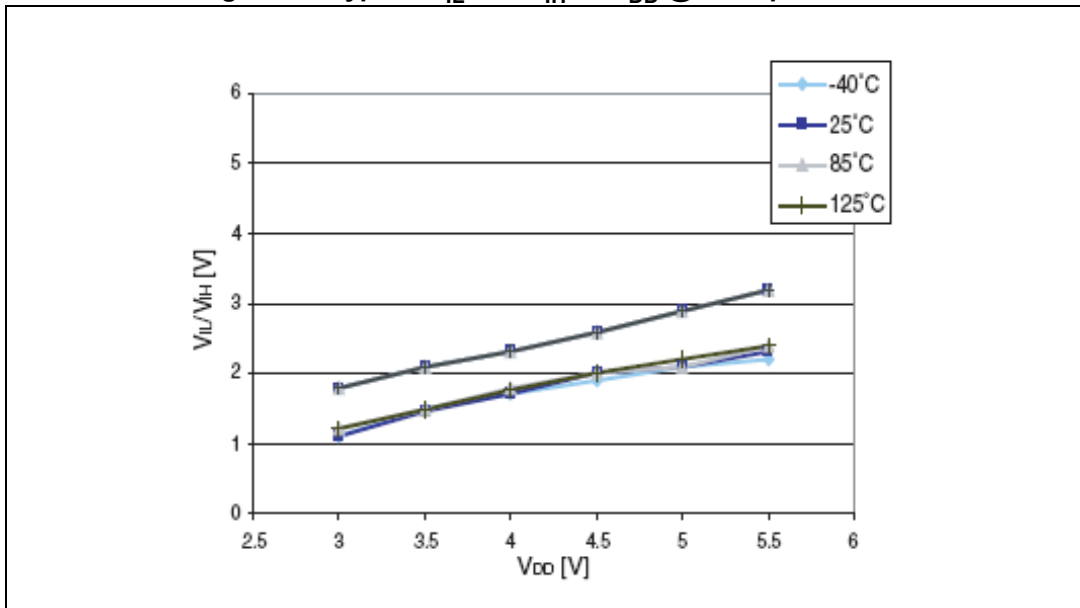


Figure 19. Typical pull-up resistance vs V_{DD} @ 4 temperatures

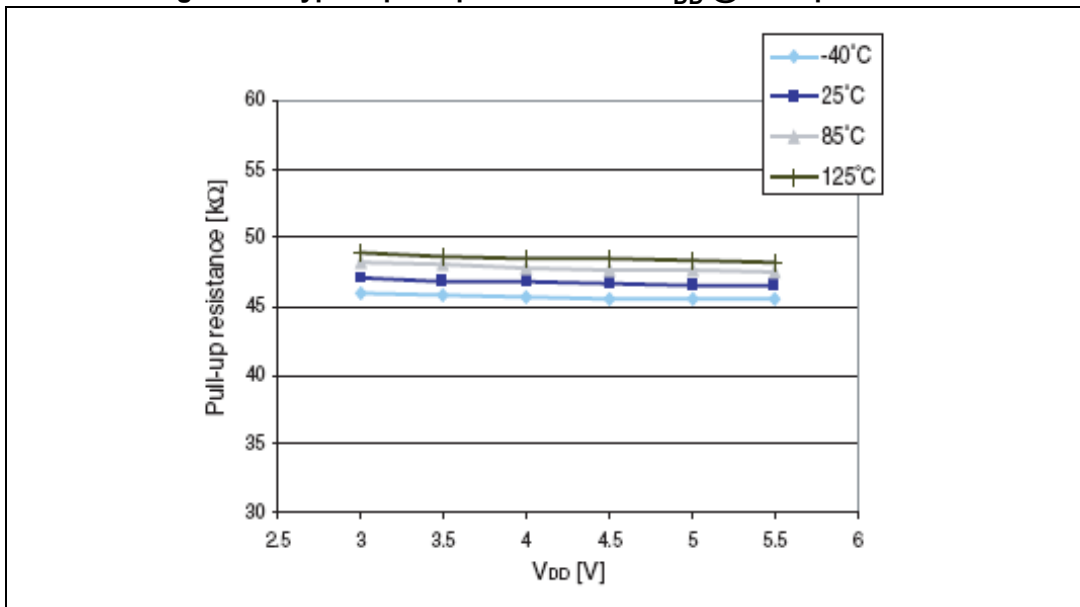
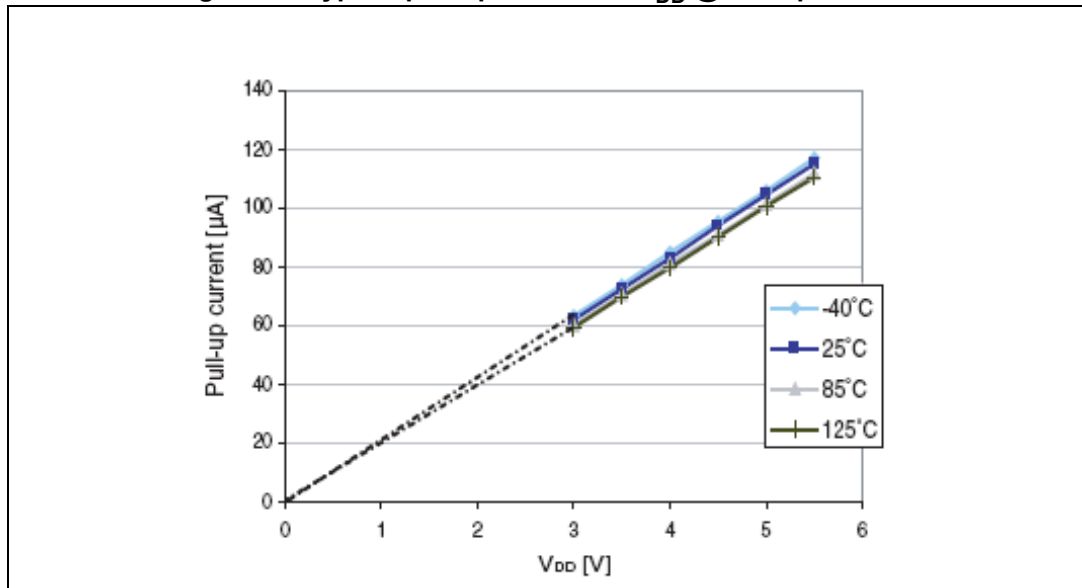


Figure 20. Typical pull-up current vs V_{DD} @ 4 temperatures



1. The pull-up is a pure resistor (slope goes through 0).

Table 36. Output driving current (standard ports)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|---------------------------------------|---|--------------------|------------------|------|
| V_{OL} | Output low level with 8 pins sunk | $I_{IO} = 10 \text{ mA}, V_{DD} = 5 \text{ V}$ | - | 2 | V |
| | Output low level with 4 pins sunk | $I_{IO} = 4 \text{ mA}, V_{DD} = 3.3 \text{ V}$ | - | 1 ⁽¹⁾ | |
| V_{OH} | Output high level with 8 pins sourced | $I_{IO} = 10 \text{ mA}, V_{DD} = 5 \text{ V}$ | 2.8 | - | V |
| | Output high level with 4 pins sourced | $I_{IO} = 4 \text{ mA}, V_{DD} = 3.3 \text{ V}$ | 2.1 ⁽¹⁾ | - | |

1. Guaranteed by characterization results.

Table 37. Output driving current (true open drain ports)

| Symbol | Parameter | Conditions | Max | Unit |
|----------|-----------------------------------|--|--------------------|------|
| V_{OL} | Output low level with 2 pins sunk | $I_{IO} = 10 \text{ mA}, V_{DD} = 5 \text{ V}$ | 1 | V |
| | | $I_{IO} = 10 \text{ mA}, V_{DD} = 3.3 \text{ V}$ | 1.5 ⁽¹⁾ | |
| | | $I_{IO} = 20 \text{ mA}, V_{DD} = 5 \text{ V}$ | 2 ⁽¹⁾ | |

1. Guaranteed by characterization results.

Table 38. Output driving current (high sink ports)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|---------------------------------------|--|--------------------|--------------------|------|
| V _{OL} | Output low level with 8 pins sunk | I _{IO} = 10 mA, V _{DD} = 5 V | - | 0.8 | V |
| | Output low level with 4 pins sunk | I _{IO} = 10 mA, V _{DD} = 3.3 V | - | 1.0 ⁽¹⁾ | |
| | Output low level with 4 pins sunk | I _{IO} = 20 mA, V _{DD} = 5 V | - | 1.5 ⁽¹⁾ | |
| V _{OH} | Output high level with 8 pins sourced | I _{IO} = 10 mA, V _{DD} = 5 V | 4.0 | - | |
| | Output high level with 4 pins sourced | I _{IO} = 10 mA, V _{DD} = 3.3 V | 2.1 ⁽¹⁾ | - | |
| | Output high level with 4 pins sourced | I _{IO} = 20 mA, V _{DD} = 5 V | 3.3 ⁽¹⁾ | - | |

1. Guaranteed by characterization results.

Typical output level curves

Figure 22 to Figure 29 show typical output level curves measured with output on a single pin.

Figure 21. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)

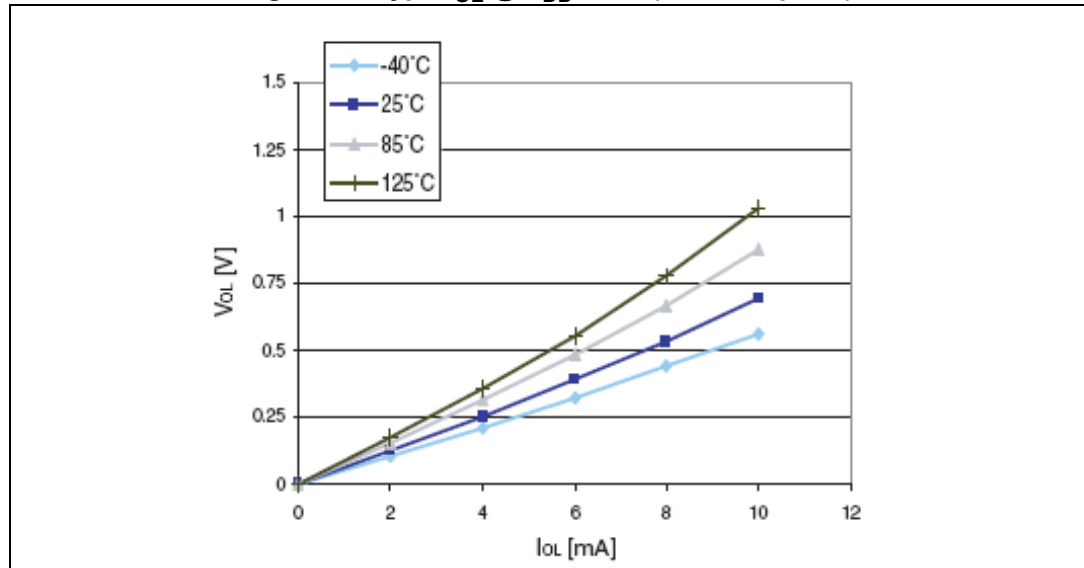


Figure 22. Typ. V_{OL} @ $V_{DD} = 3.3$ V (standard ports)

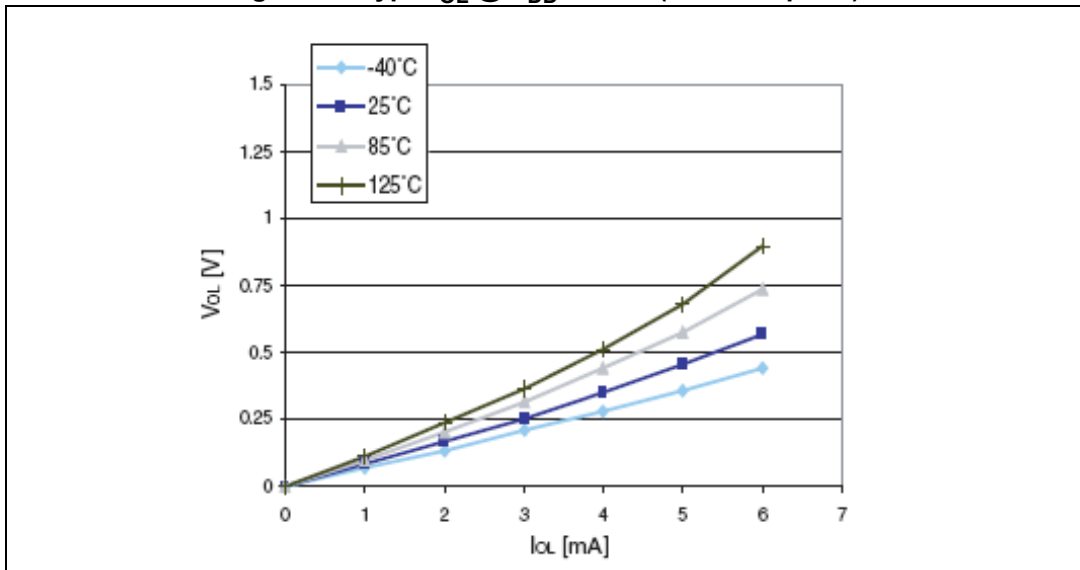


Figure 23. Typ. V_{OL} @ $V_{DD} = 5$ V (true open drain ports)

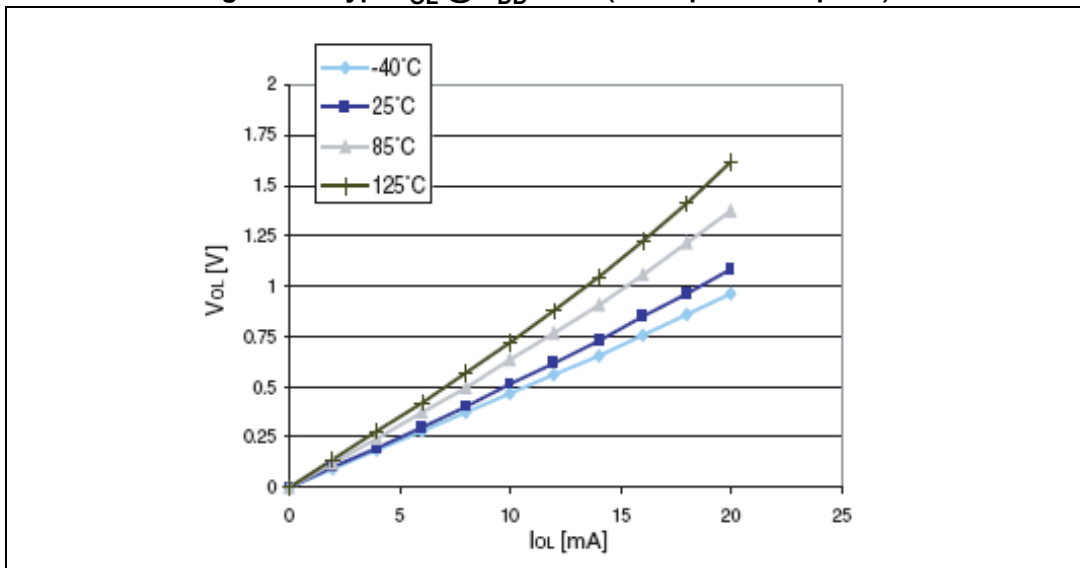


Figure 24. Typ. V_{OL} @ $V_{DD} = 3.3$ V (true open drain ports)

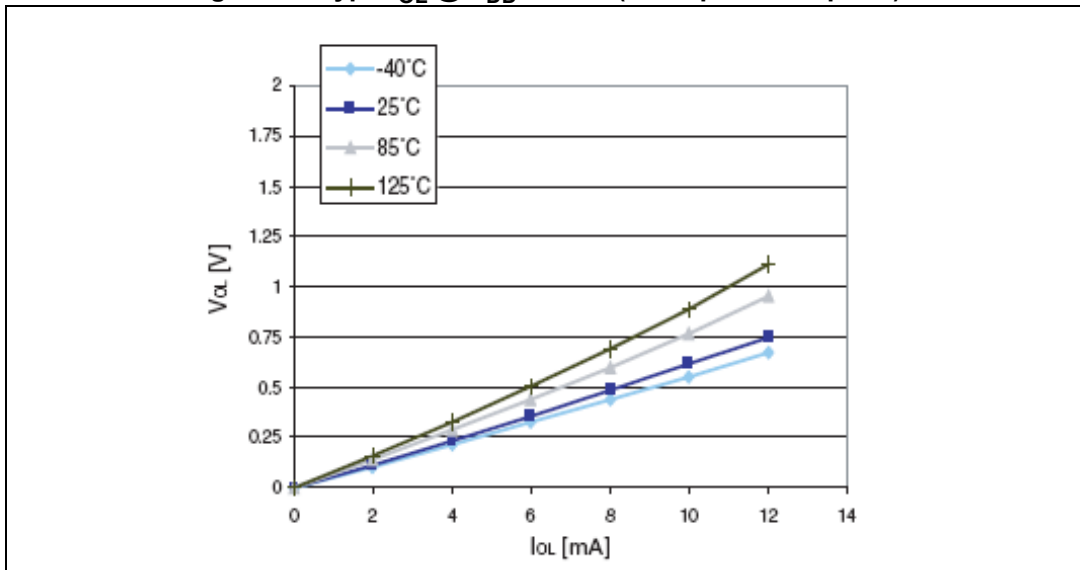


Figure 25. Typ. V_{OL} @ $V_{DD} = 5$ V (high sink ports)

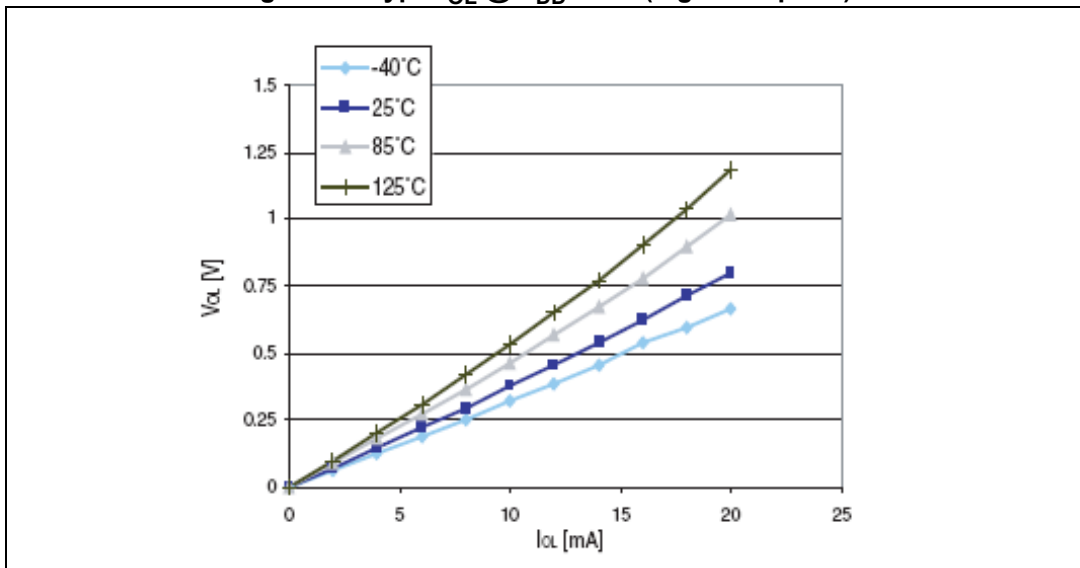


Figure 26. Typ. V_{OL} @ $V_{DD} = 3.3$ V (high sink ports)

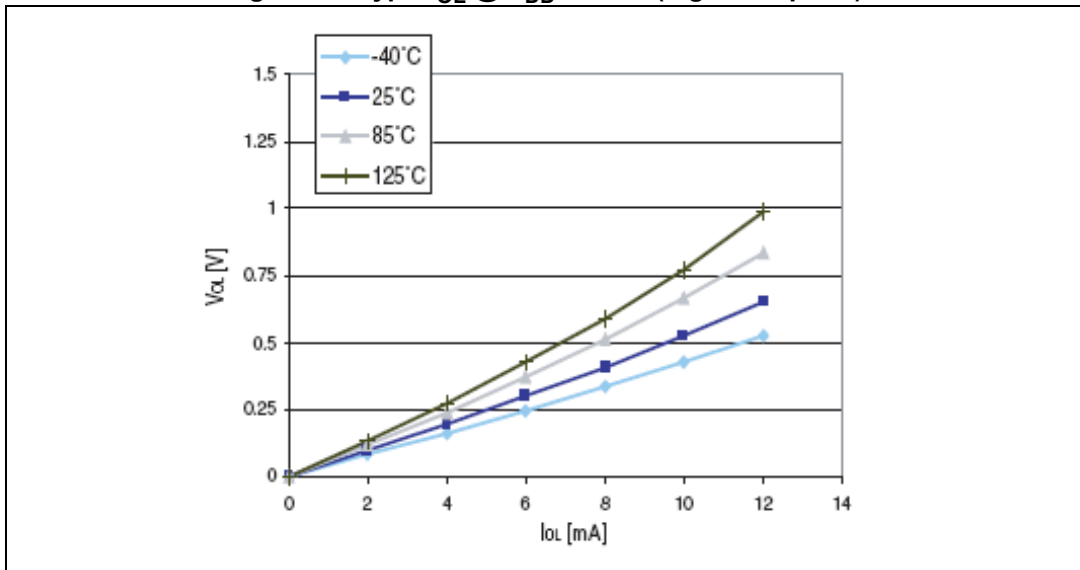


Figure 27. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5$ V (standard ports)

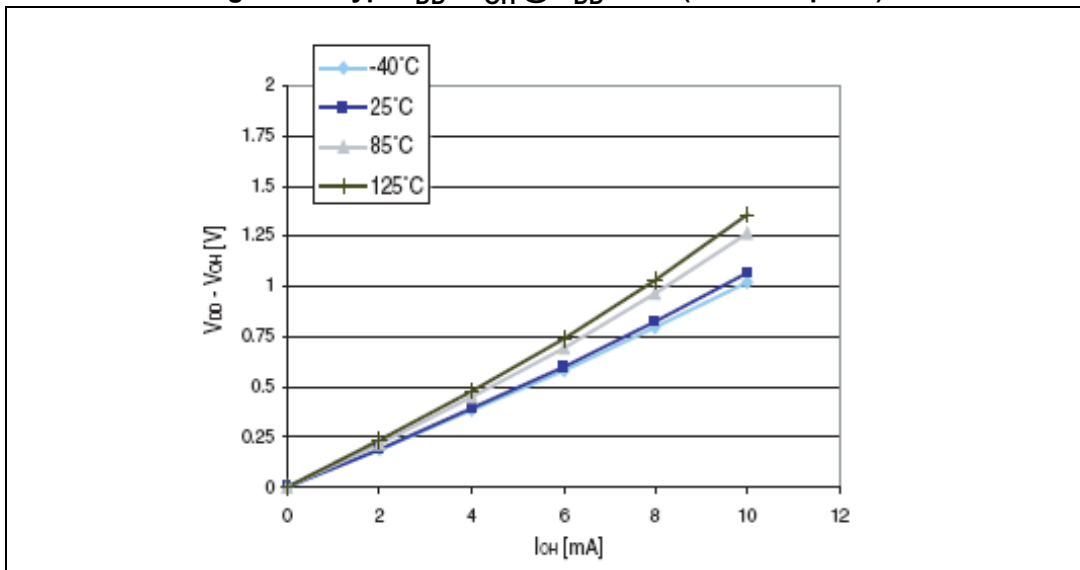


Figure 28. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3\text{ V}$ (standard ports)

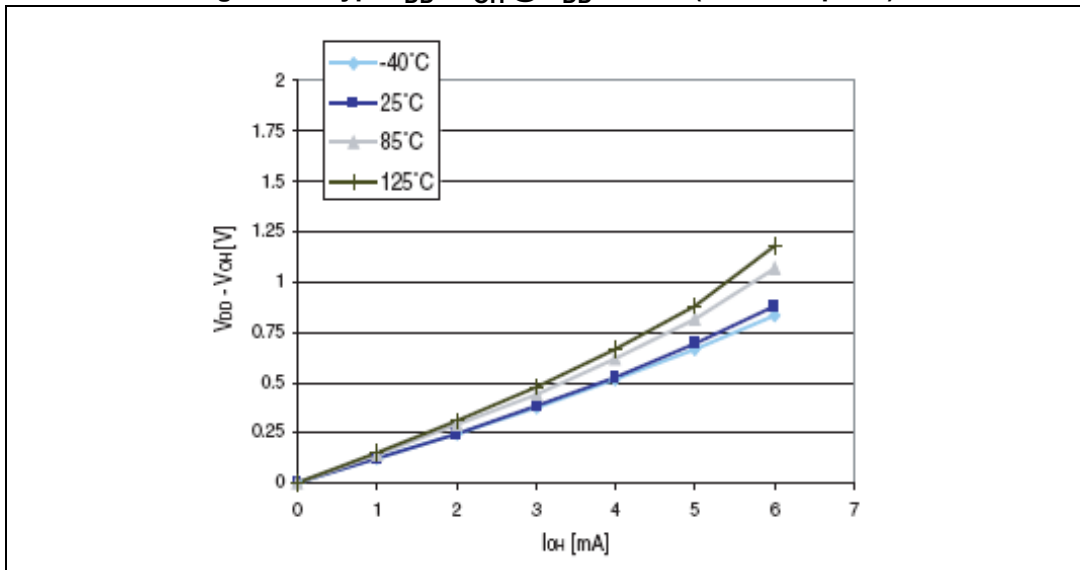


Figure 29. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5\text{ V}$ (high sink ports)

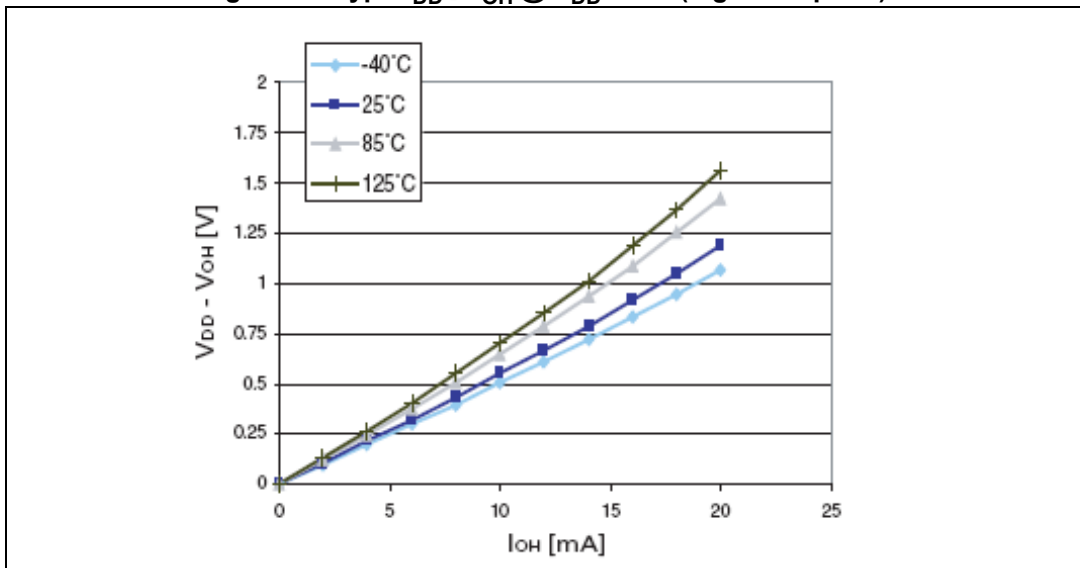
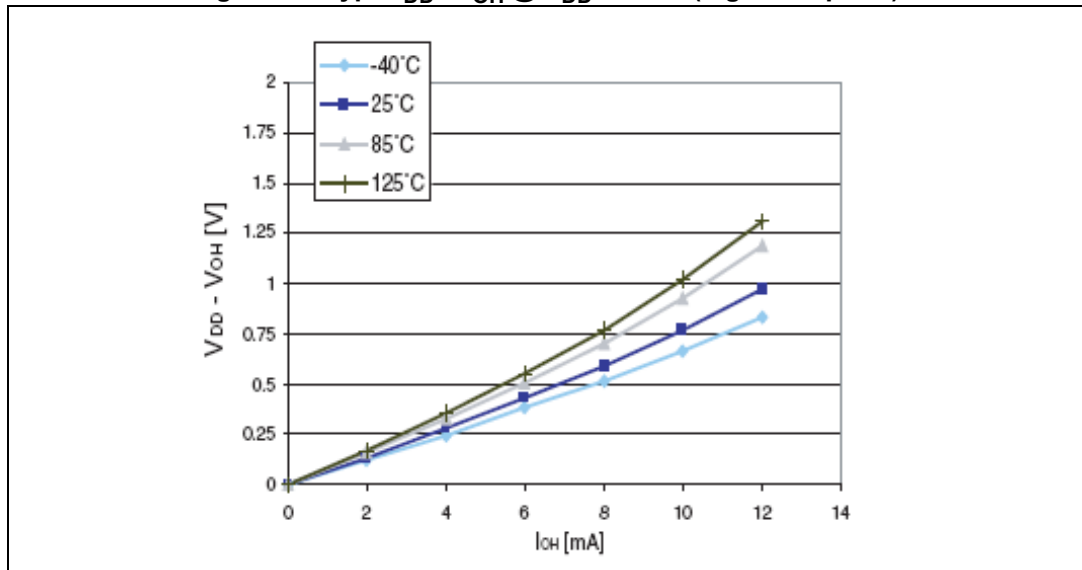


Figure 30. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3$ V (high sink ports)



9.3.7 SPI serial peripheral interface

Unless otherwise specified, the parameters given in [Table 39](#) are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 39. SPI characteristics

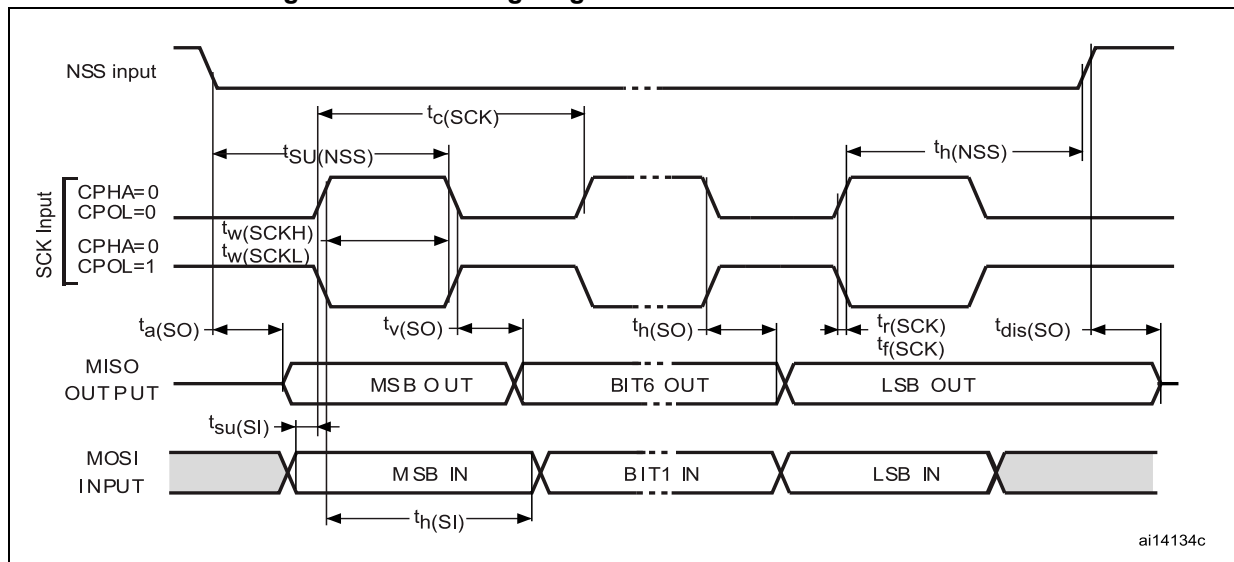
| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|---------------------|-------------|-----|-----|------|
| f_{SCK} $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 7 | |

Table 39. SPI characteristics (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|------------------------------|---------------------------------|-----------------------|-----------------------|------|
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 25 | ns |
| $t_{su(NSS)}^{(1)}$ | NSS setup time | Slave mode | $4 \times t_{MASTER}$ | - | |
| $t_{h(NSS)}^{(1)}$ | NSS hold time | Slave mode | 70 | - | |
| $t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$ | SCK high and low time | Master mode | $t_{SCK}/2 - 15$ | $t_{SCK}/2 + 15$ | |
| $t_{su(MI)}^{(1)}$ $t_{su(SI)}^{(1)}$ | Data input setup time | Master mode | 5 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}^{(1)}$ $t_{h(SI)}^{(1)}$ | Data input hold time | Master mode | 7 | - | |
| | | Slave mode | 10 | - | |
| $t_{a(SO)}^{(1)(2)}$ | Data output access time | Slave mode | - | $3 \times t_{MASTER}$ | |
| $t_{dis(SO)}^{(1)(3)}$ | Data output disable time | Slave mode | 25 | - | |
| $t_{v(SO)}^{(1)}$ | Data output valid time | Slave mode (after enable edge) | - | 65 | |
| $t_{v(MO)}^{(1)}$ | Data output valid time | Master mode (after enable edge) | - | 30 | |
| $t_{h(SO)}^{(1)}$ | Data output hold time | Slave mode (after enable edge) | 27 | - | |
| $t_{h(MO)}^{(1)}$ | | Master mode (after enable edge) | 11 | - | |

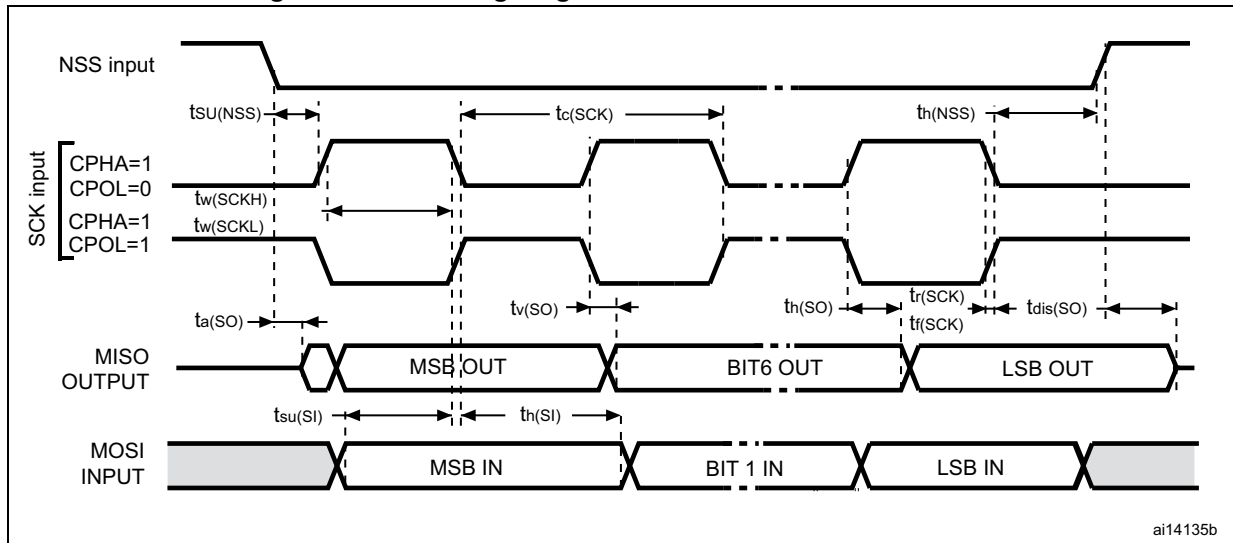
1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 31. SPI timing diagram - slave mode and CPHA = 0



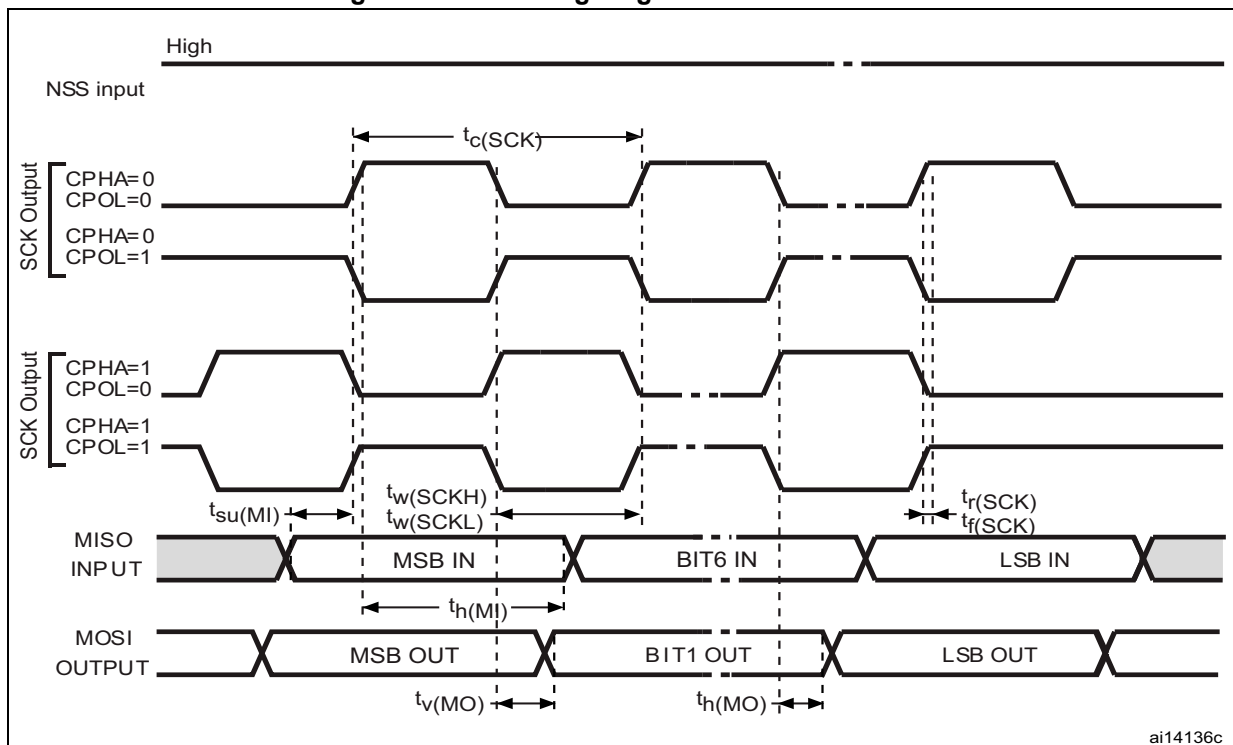
ai14134c

Figure 32. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 33. SPI timing diagram - master mode⁽¹⁾



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

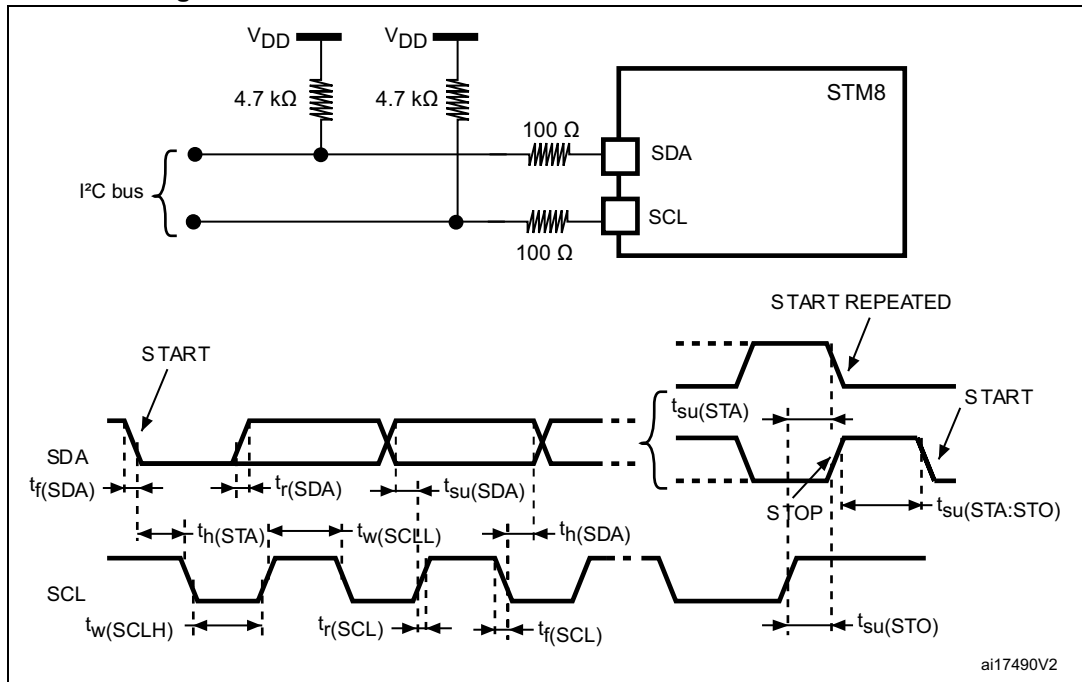
9.3.8 I2C interface characteristics

Table 40. I2C characteristics

| Symbol | Parameter | Standard mode I2C | | Fast mode I2C ⁽¹⁾ | | Unit |
|------------------------------|---|--------------------|--------------------|------------------------------|--------------------|---------------|
| | | Min ⁽²⁾ | Max ⁽²⁾ | Min ⁽²⁾ | Max ⁽²⁾ | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | μs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 ⁽³⁾ | - | 0 ⁽⁴⁾ | 900 ⁽³⁾ | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | μs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | μs |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | μs |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | μs |
| C_b | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. f_{MASTER} must be at least 8 MHz to achieve max fast I2C speed (400 kHz)
2. Data based on standard I2C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Figure 34. Typical application with I2C bus and timing diagram



1. Measurement points are made at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$

9.3.9 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA} , f_{MASTER} , and T_A unless otherwise specified.

Table 41. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--|----------------------------|----------|------|----------|-------------|
| f_{ADC} | ADC clock frequency | $V_{DDA} = 3$ to 5.5 V | 1 | - | 4 | MHz |
| | | $V_{DDA} = 4.5$ to 5.5 V | 1 | - | 6 | |
| V_{AIN} | Conversion voltage range ⁽¹⁾ | - | V_{SS} | - | V_{DD} | V |
| C_{ADC} | Internal sample and hold capacitor | - | - | 3 | - | pF |
| $t_S^{(1)}$ | Sampling time | $f_{ADC} = 4$ MHz | - | 0.75 | - | μs |
| | | $f_{ADC} = 6$ MHz | - | 0.5 | - | |
| t_{STAB} | Wakeup time from standby | - | - | 7 | - | μs |
| t_{CONV} | Total conversion time (including sampling time, 10-bit resolution) | $f_{ADC} = 4$ MHz | 3.5 | | | μs |
| | | $f_{ADC} = 6$ MHz | 2.33 | | | μs |
| | | - | 14 | | | $1/f_{ADC}$ |

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 42. ADC accuracy with $R_{AIN} < 10$ kΩ, $V_{DD} = 5$ V

| Symbol | Parameter | Conditions | Typ | Max ⁽¹⁾ | Unit |
|---------|---|-------------------|-----|--------------------|------|
| $ E_T $ | Total unadjusted error ⁽²⁾ | $f_{ADC} = 2$ MHz | 1.6 | 3.5 | LSB |
| | | $f_{ADC} = 4$ MHz | 2.2 | 4 | |
| | | $f_{ADC} = 6$ MHz | 2.4 | 4.5 | |
| $ E_O $ | Offset error ⁽²⁾ | $f_{ADC} = 2$ MHz | 1.1 | 2.5 | |
| | | $f_{ADC} = 4$ MHz | 1.5 | 3 | |
| | | $f_{ADC} = 6$ MHz | 1.8 | 3 | |
| $ E_G $ | Gain error ⁽²⁾ | $f_{ADC} = 2$ MHz | 1.5 | 3 | |
| | | $f_{ADC} = 4$ MHz | 2.1 | 3 | |
| | | $f_{ADC} = 6$ MHz | 2.2 | 4 | |
| $ E_D $ | Differential linearity error ⁽²⁾ | $f_{ADC} = 2$ MHz | 0.7 | 1.5 | |
| | | $f_{ADC} = 4$ MHz | 0.7 | 1.5 | |
| | | $f_{ADC} = 6$ MHz | 0.7 | 1.5 | |
| $ E_L $ | Integral linearity error ⁽²⁾ | $f_{ADC} = 2$ MHz | 0.6 | 1.5 | |
| | | $f_{ADC} = 4$ MHz | 0.8 | 2 | |
| | | $f_{ADC} = 6$ MHz | 0.8 | 2 | |

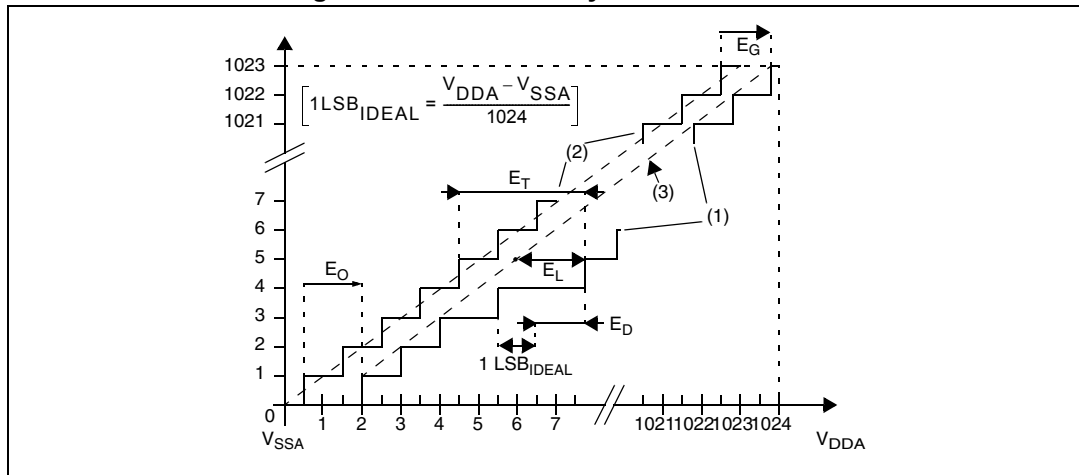
1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 9.3.6](#) does not affect the ADC accuracy.

Table 43. ADC accuracy with $R_{AIN} < 10\text{ k}\Omega$, R_{AIN} , $V_{DD} = 3.3\text{ V}$

| Symbol | Parameter | Conditions | Typ | Max ⁽¹⁾ | Unit |
|----------------|---|--------------------------|-----|--------------------|------|
| E _T | Total unadjusted error ⁽²⁾ | f _{ADC} = 2 MHz | 1.6 | 3.5 | LSB |
| | | f _{ADC} = 4 MHz | 1.9 | 4 | |
| E _O | Offset error ⁽²⁾ | f _{ADC} = 2 MHz | 1 | 2.5 | |
| | | f _{ADC} = 4 MHz | 1.5 | 2.5 | |
| E _G | Gain error ⁽²⁾ | f _{ADC} = 2 MHz | 1.3 | 3 | |
| | | f _{ADC} = 4 MHz | 2 | 3 | |
| E _D | Differential linearity error ⁽²⁾ | f _{ADC} = 2 MHz | 0.7 | 1.0 | |
| | | f _{ADC} = 4 MHz | 0.7 | 1.5 | |
| E _L | Integral linearity error ⁽²⁾ | f _{ADC} = 2 MHz | 0.6 | 1.5 | |
| | | f _{ADC} = 4 MHz | 0.8 | 2 | |

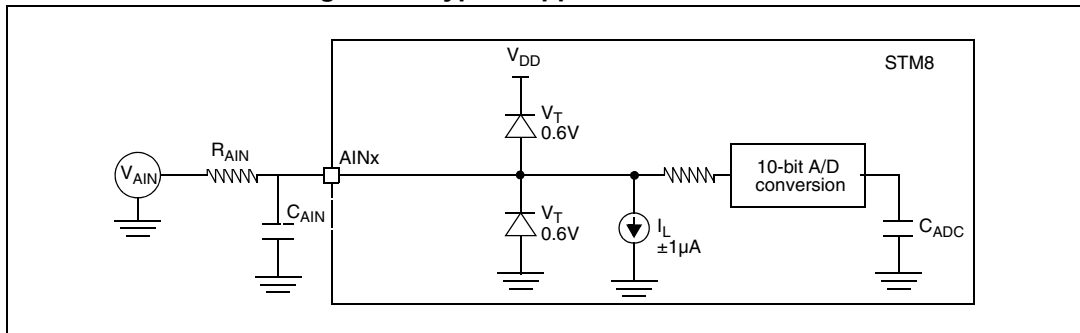
1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 9.3.6](#) does not affect the ADC accuracy.

Figure 35. ADC accuracy characteristics



1. Example of an actual transfer curve.
 2. The ideal transfer curve
 3. End point correlation line
- E_T** = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset error: deviation between the first actual transition and the first ideal one.
 E_G = Gain error: deviation between the last ideal transition and the last actual one.
 E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
 E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 36. Typical application with ADC



9.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 44. EMS data

| Symbol | Parameter | Conditions | Level/class |
|------------|--|---|--------------------|
| V_{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{MASTER} = 16\text{ MHz}$, conforming to IEC 61000-4-2 | TBD ⁽¹⁾ |
| V_{EFTB} | Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{MASTER} = 16\text{ MHz}$, conforming to IEC 61000-4-4 | TBD ⁽¹⁾ |

1. Data obtained with HSI clock configuration, after applying HW recommendations described in AN2860 - EMC guidelines for STM8Smicrocontrollers.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling two LEDs through the I/O ports), the product is monitored in terms of emission. Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 45. EMI data

| Symbol | Parameter | Conditions | | | | Unit |
|-----------|------------|--|--------------------------|-----------------------------|----------------|------------|
| | | General conditions | Monitored frequency band | Max $f_{HSE}/f_{CPU}^{(1)}$ | | |
| | | | | 16 MHz/ 8 MHz | 16 MHz/ 16 MHz | |
| S_{EMI} | Peak level | $V_{DD} = 5 V$ $T_A = 25 ^\circ C$ SO8N package conforming to IEC 61967-2 | 0.1 MHz to 30 MHz | TBD | TBD | dB μ V |
| | | | 30 MHz to 130 MHz | TBD | TBD | |
| | | | 130 MHz to 1 GHz | TBD | TBD | |
| | EMI level | - | TBD | TBD | - | |

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (one positive then one negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: the Human Body Model (HBM). This test conforms to the JESD22-A114/A115A standard. For more details, refer to the application note AN1181.

Table 46. ESD absolute maximum ratings

| Symbol | Ratings | Conditions | Class | Maximum value ⁽¹⁾ | Unit |
|----------------|---|--|-------|------------------------------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (Human body model) | $T_A = 25^\circ C$, conforming to JESD22-A114 | A | TBD | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (Charge device model) | $T_A = 25^\circ C$, conforming to JESD22-C101 | IV | TBD | V |

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) is performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 47. Electrical sensitivities

| Symbol | Parameter | Conditions | Class ⁽¹⁾ |
|--------|-----------------------|------------------------|----------------------|
| LU | Static latch-up class | T _A = 25 °C | TBD |
| | | T _A = 85 °C | TBD |

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

10 Package information

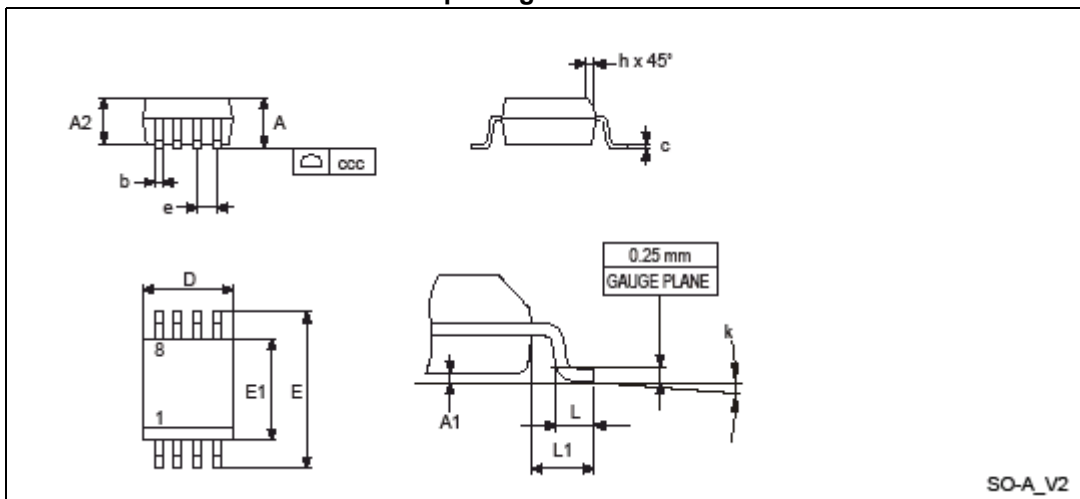
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Failure analysis and guarantee

The small number of pins available induces limitations on failure analysis depth in case of isolated symptoms, typically with an impact lower than 0.1%. Please contact your sales office for additional information for any failure analysis. STMicroelectronics will make a feasibility study for investigation based on failure rate and symptom description prior to responsibility endorsement.

10.1 SO8N package information

Figure 37. SO8N – 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package outline



1. Drawing not to scale.

Table 48. SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, package mechanical data

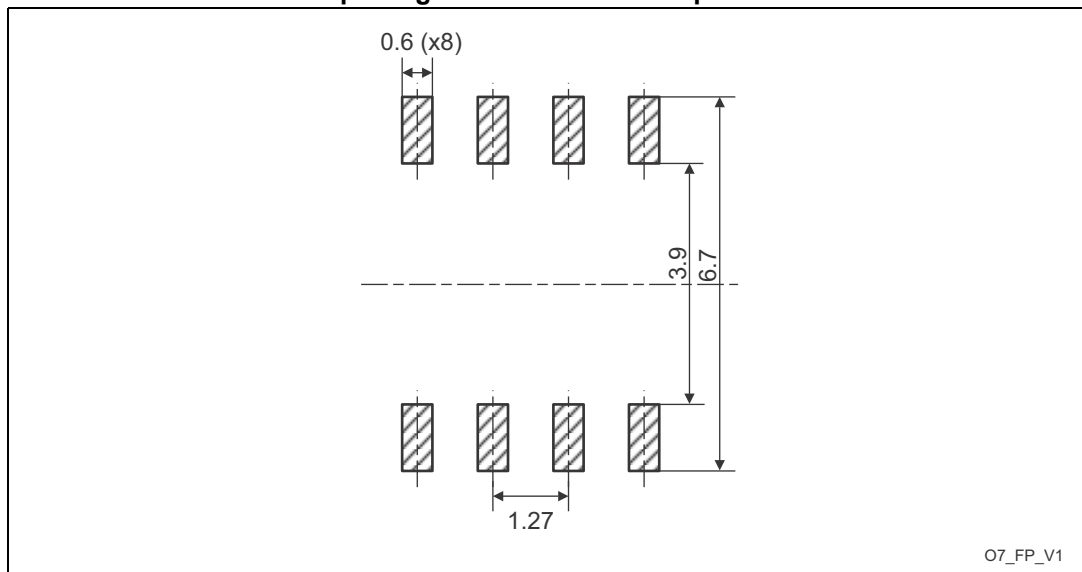
| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|------|-------|-----------------------|------|--------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.750 | - | - | 0.0689 |
| A1 | 0.100 | - | 0.250 | 0.0039 | - | 0.0098 |
| A2 | 1.250 | - | - | 0.0492 | - | - |
| b | 0.280 | - | 0.480 | 0.0110 | - | 0.0189 |
| c | 0.170 | - | 0.230 | 0.0067 | - | 0.0091 |

Table 48. SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| D | 4.800 | 4.900 | 5.000 | 0.1890 | 0.1929 | 0.1969 |
| E | 5.800 | 6.000 | 6.200 | 0.2283 | 0.2362 | 0.2441 |
| E1 | 3.800 | 3.900 | 4.000 | 0.1496 | 0.1535 | 0.1575 |
| e | - | 1.270 | - | - | 0.0500 | - |
| h | 0.250 | - | 0.500 | 0.0098 | - | 0.0197 |
| k | 0° | - | 8° | 0° | - | 8° |
| L | 0.400 | - | 1.270 | 0.0157 | - | 0.0500 |
| L1 | - | 1.040 | - | - | 0.0409 | - |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 38. SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, package recommended footprint

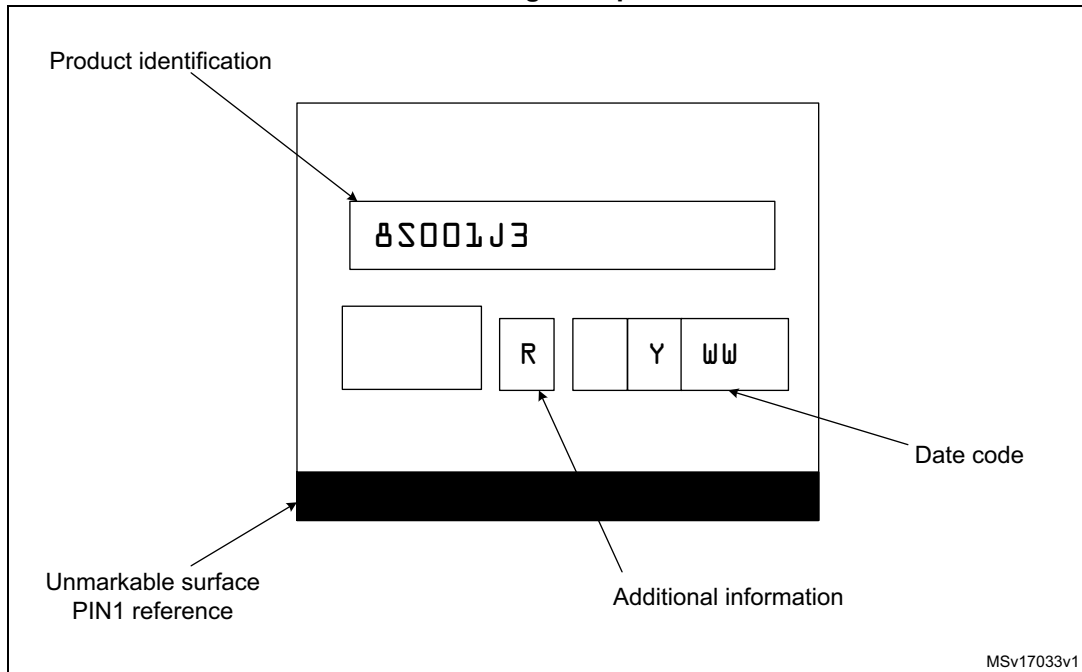


Device marking for SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width

The following figure gives an example of topside marking orientation versus pin 1/ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 39. SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width, marking example



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

10.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 17: General operating conditions](#).

The maximum chip-junction temperature, T_{Jmax} , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins, where:
 $P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma ((V_{DD} - V_{OH}) * I_{OH})$, and taking account of the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 49. Thermal characteristics⁽¹⁾

| Symbol | Parameter | Value | Unit |
|---------------|---|-------|------|
| θ_{JA} | Thermal resistance junction-ambient SO8N | 102 | °C/W |

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

10.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see [Figure 40: STM8S001J3 ordering information scheme\(1\)](#)).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature $T_{Amax} = 75\text{ °C}$ (measured according to JESD51-2)
- $I_{DDmax} = 8\text{ mA}$, $V_{DD} = 5.0\text{ V}$
- Maximum 4 I/Os used at the same time in output at low level with
 $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$
 $P_{INTmax} = 8\text{ mA} \times 5.0\text{ V} = 40\text{ mW}$
 $P_{Dmax} = 40\text{ mW} + (8 \times 0.4 \times 4)\text{ mW}$
 Thus: $P_{Dmax} = 52.8\text{ mW}$

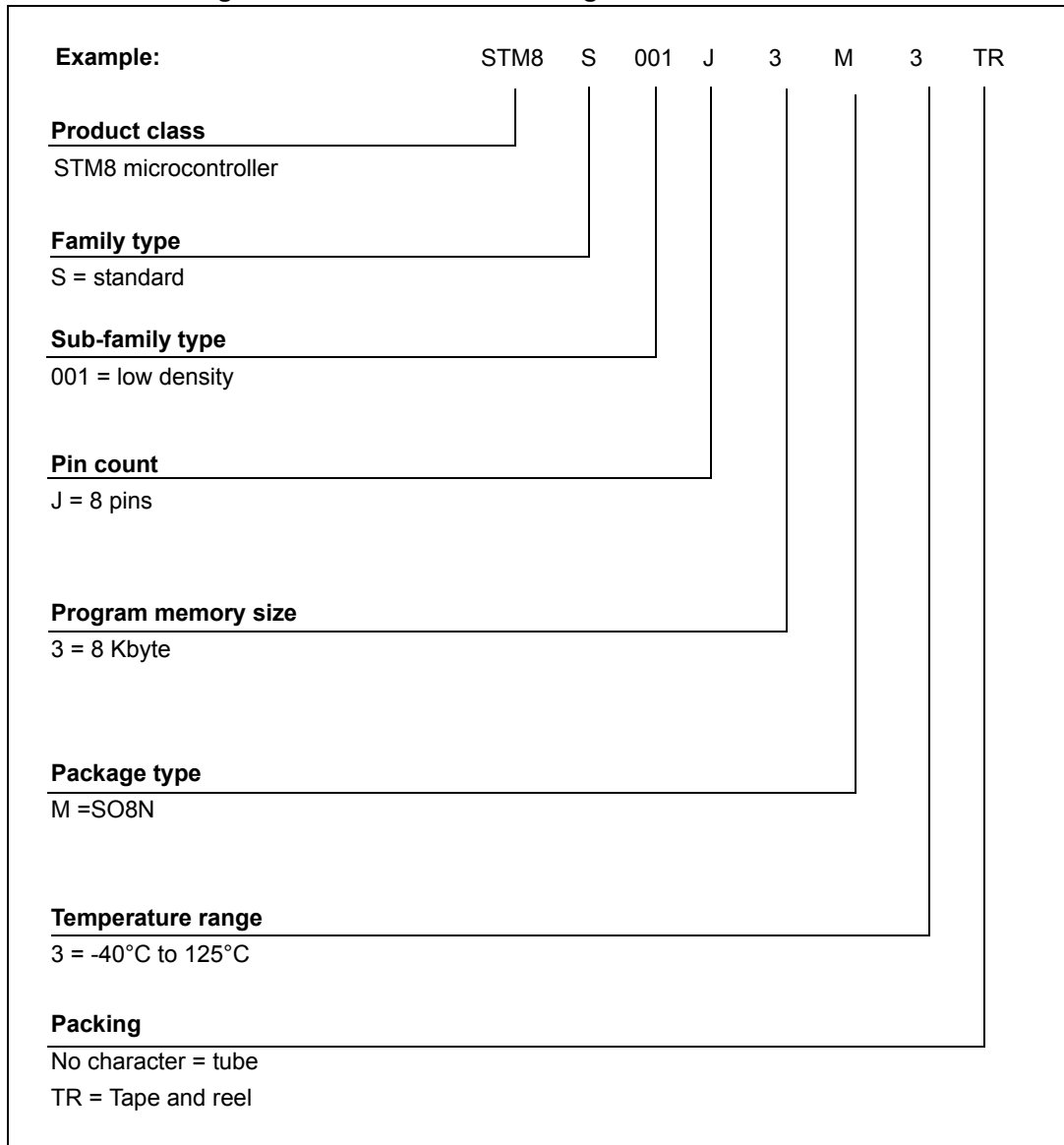
Using the values obtained in [Section Table 49.: Thermal characteristics](#) T_{Jmax} is calculated as follows for SO8N package 102 °C/W :

$$T_{Jmax} = 75\text{ °C} + (102\text{ °C/W} \times 52.8\text{ mW}) = 75\text{ °C} + 5.4\text{ °C} = 80.4\text{ °C}.$$

Above information is within the range ($-40 < T_J < 130\text{ °C}$)

11 Ordering information

Figure 40. STM8S001J3 ordering information scheme⁽¹⁾



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the ST Sales Office nearest to you.

12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components users need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STIce such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify the user STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- **Cosmic C compiler for STM8** – One free version that outputs up to Kbytes of code is available. For more information, see www.cosmic-software.com.
- **Raisonance C compiler for STM8** – One free version that outputs up to Kbytes of code. For more information, see www.raisonance.com.
- **STM8 assembler linker** – Free assembly toolchain included in the STVD toolset, which allows users to assemble and link the user application source code.

12.3 Programming tools

During the development cycle, STIce provides in-circuit programming of the STM8 Flash microcontroller on user application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the user STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

13 Revision history

Table 50. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 24-May-2017 | 1 | Initial release. |
| 29-Jun-2017 | 2 | Updated: <i>Section 10: Package information</i> <i>Figure 3: STM8S001J3 SO8N pinout</i> <i>Table 5: STM8S001J3 pin description</i> <i>Table 13: STM8S001J3 alternate function remapping bits for 8-pin devices</i> Added: <i>Section : Device marking for SO8N – 8-lead 4.9 x 6 mm, plastic small outline, 150 mils body width</i> |

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved