# DMOS FULL-BRIDGE MOTOR DRIVERS

## FEATURES

- **Low ON-Resistance [$R_{ds(ON)}$] Outputs**
- **Overcurrent Protection**
- **Motor Lead Short-to-Supply Protection**
- **Short-to-Ground Protection**
- **Low-Power Mode**
- **Synchronous Rectification**
- **Diagnostic Output**
- **Internal Undervoltage Lockout (UVLO)**

- **Crossover-Current Protection**
- **16-Pin QFN With PowerPAD™ Package**

## APPLICATIONS

- **Printers**
- **Industrial Automation**

## DESCRIPTION/ORDERING INFORMATION

Designed to control dc motors by using pulse width modulation (PWM), the DRV8800/DRV8801 is capable of peak output currents up to ±2.8 A and operating voltages up to 36 V.

The PHASE and ENABLE inputs provide dc motor speed and direction control by applying external pulse-width modulation (PWM) and control signals. Internal synchronous rectification control circuitry provides lower power dissipation during PWM operation.

Internal circuit protection includes motor lead short-to-supply/short-to-ground, thermal shutdown with hysteresis, undervoltage monitoring of VBB and VCP, and crossover-current protection.

The DRV8800/DRV8801 is supplied in a thin-profile 16-pin QFN (RTY) PowerPAD™ package, providing enhanced thermal dissipation. The devices are lead free (Pb free).

### ORDERING INFORMATION

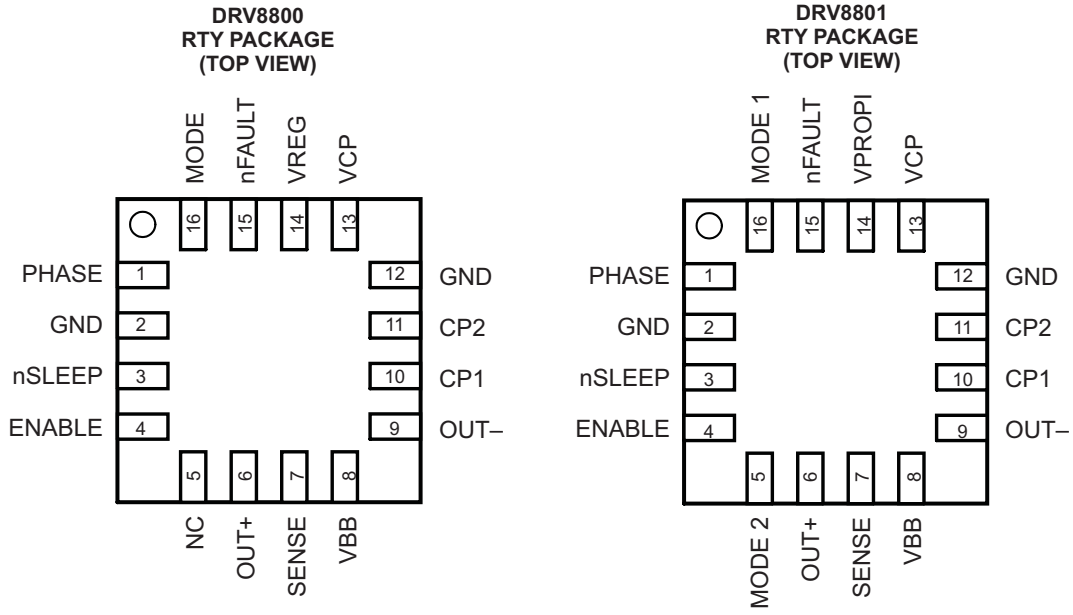| $T_A$ | PACKAGE[1][2] | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| −20°C to 80°C | Plastic QFN 16 (S-PQFP-16) – RTY | DRV8800RTYR | DRV8800A0RTY |
| | | DRV8800RTYT | DRV8800A0RTY |
| | | DRV8801RTYR | DRV8801A0RTY |
| | | DRV8801RTYT | DRV8801A0RTY |

(1)  For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2)  Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

**DRV8800**
**RTY PACKAGE**
**(TOP VIEW)**

MODE  nFAULT  VREG  VCP
16  15  14  13

PHASE 1 ... 12 GND
GND 2 ... 11 CP2
nSLEEP 3 ... 10 CP1
ENABLE 4 ... 9 OUT−

5  6  7  8
NC  OUT+  SENSE  VBB

**DRV8801**
**RTY PACKAGE**
**(TOP VIEW)**

MODE 1  nFAULT  VPROPI  VCP
16  15  14  13

PHASE 1 ... 12 GND
GND 2 ... 11 CP2
nSLEEP 3 ... 10 CP1
ENABLE 4 ... 9 OUT−

5  6  7  8
MODE 2  OUT+  SENSE  VBB

NC – Do not connect

## TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| | DRV8800 | DRV8801 | |
| 1 | PHASE | PHASE | Phase logic input for direction control |
| 2 | GND | GND | Ground |
| 3 | nSLEEP | nSLEEP | Sleep logic input |
| 4 | ENABLE | ENABLE | Enable logic input |
| 5 | NC | MODE 2 | No connect (DRV8800), Mode 2 logic input (DRV8801) |
| 6 | OUTA | OUTA | DMOS full-bridge output A |
| 7 | SENSE | SENSE | Sense power return |
| 8 | VBB | VBB | Load supply voltage |
| 9 | OUTB | OUTB | DMOS full-bridge output B |
| 10 | CP1 | CP1 | Charge-pump capacitor 1 |
| 11 | CP2 | CP2 | Charge-pump capacitor 2 |
| 12 | GND | GND | Ground |
| 13 | VCP | VCP | Reservoir capacitor |
| 14 | VREG | VPROPI | Regulated voltage (DRV8800), Winding current proportional voltage output (DRV8801) |
| 15 | nFAULT | nFAULT | Fault open-drain output |
| 16 | MODE | MODE 1 | Mode logic input |
| | PowerPAD | PowerPAD | Exposed pad for thermal dissipation connect to GND pins |

**DRV8800 TYPICAL APPLICATION DIAGRAM**
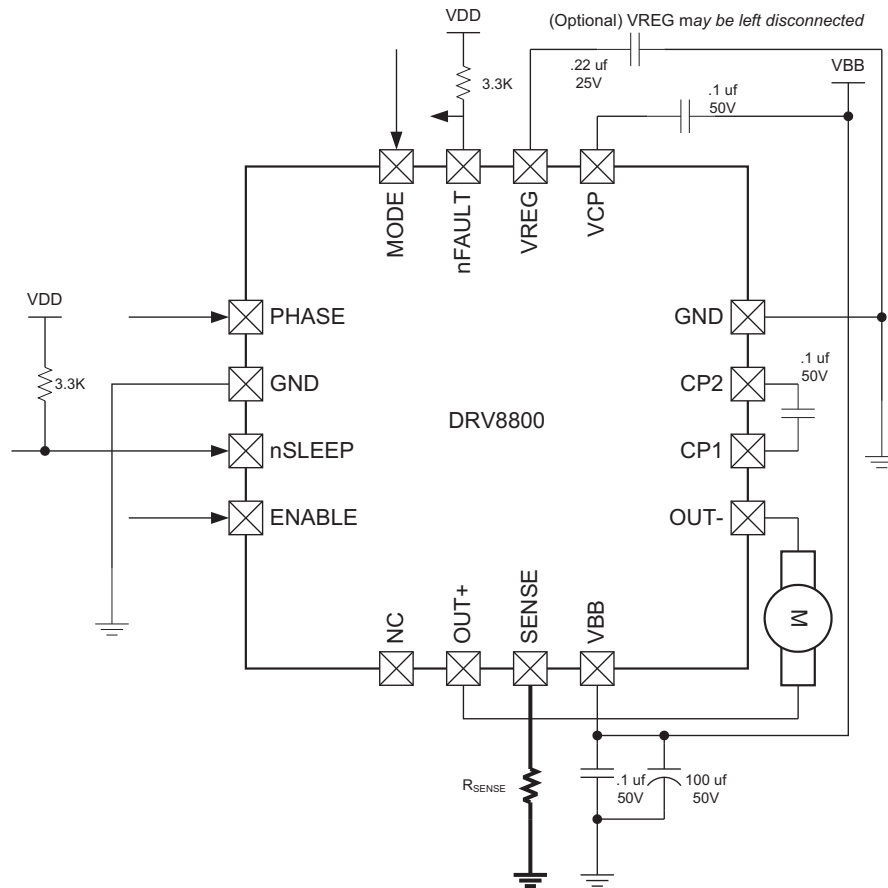
## DRV8801 TYPICAL APPLICATION DIAGRAM
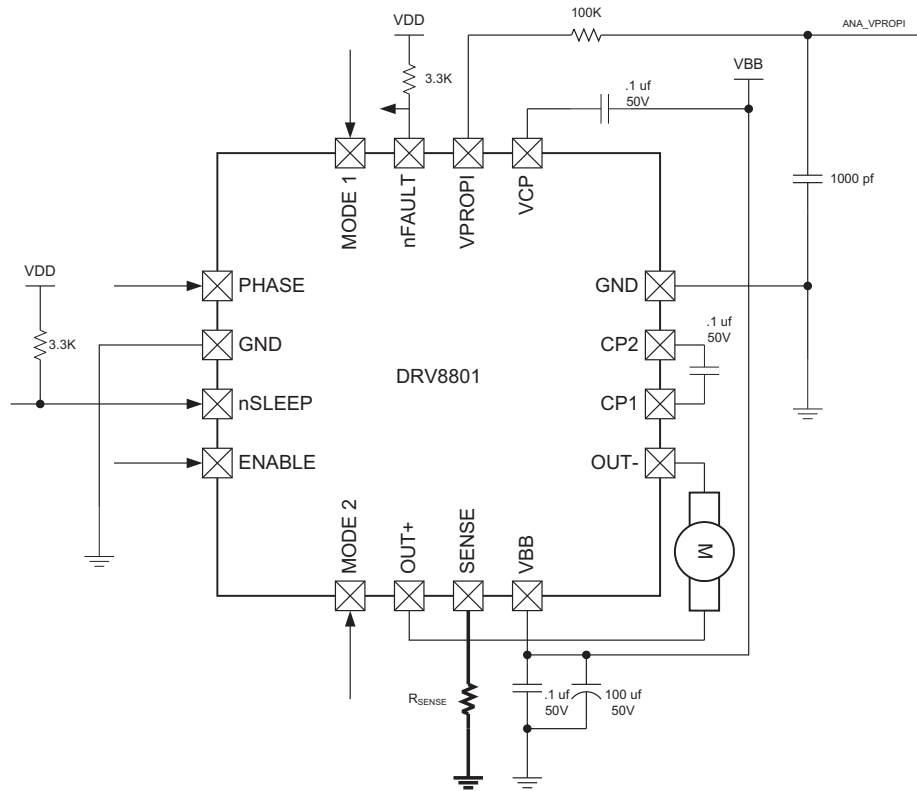
**DRV8800 FUNCTIONAL BLOCK DIAGRAM**

Product Folder Link(s): *DRV8800 DRV8801*
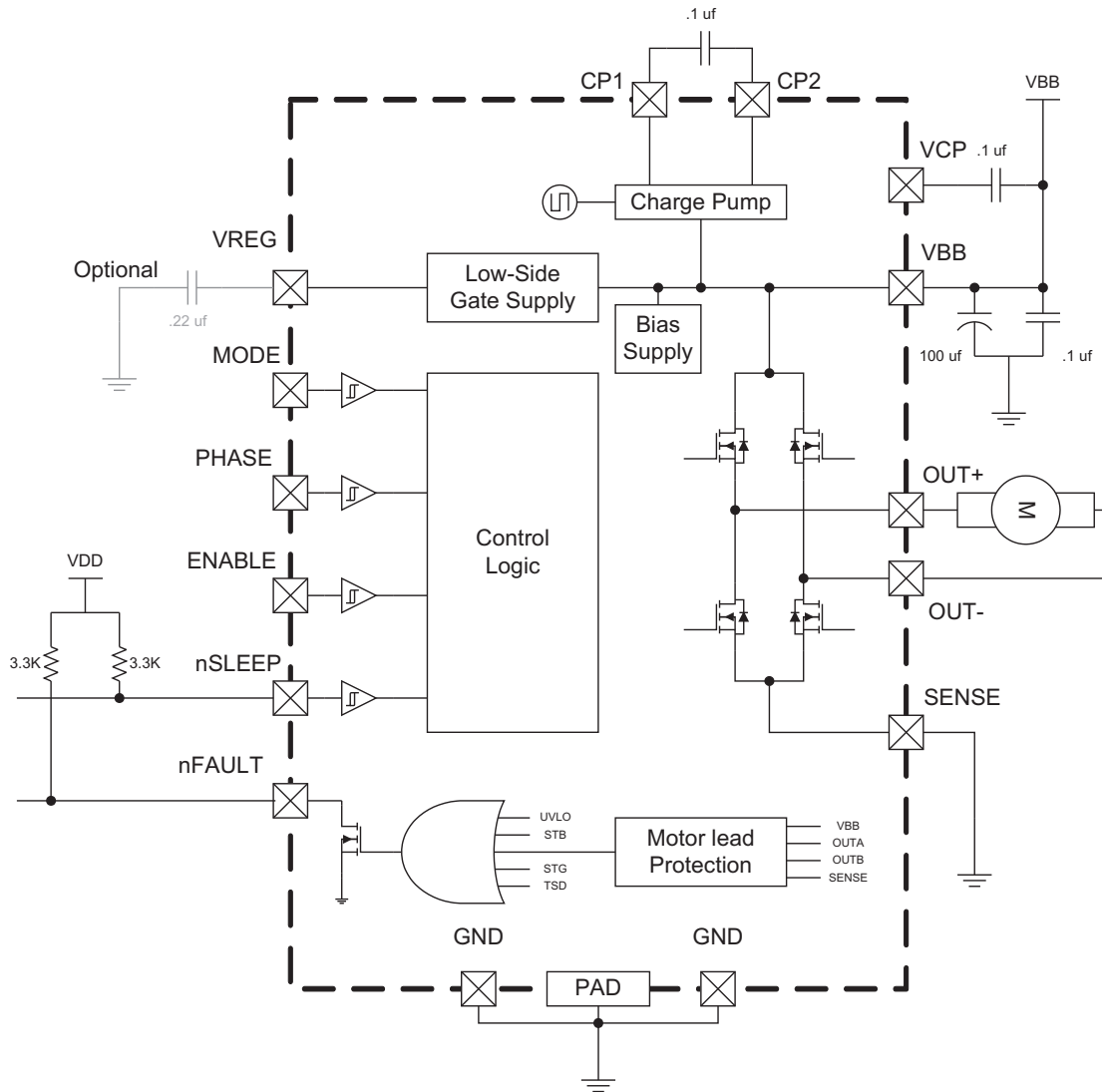
## DRV8801 FUNCTIONAL BLOCK DIAGRAM
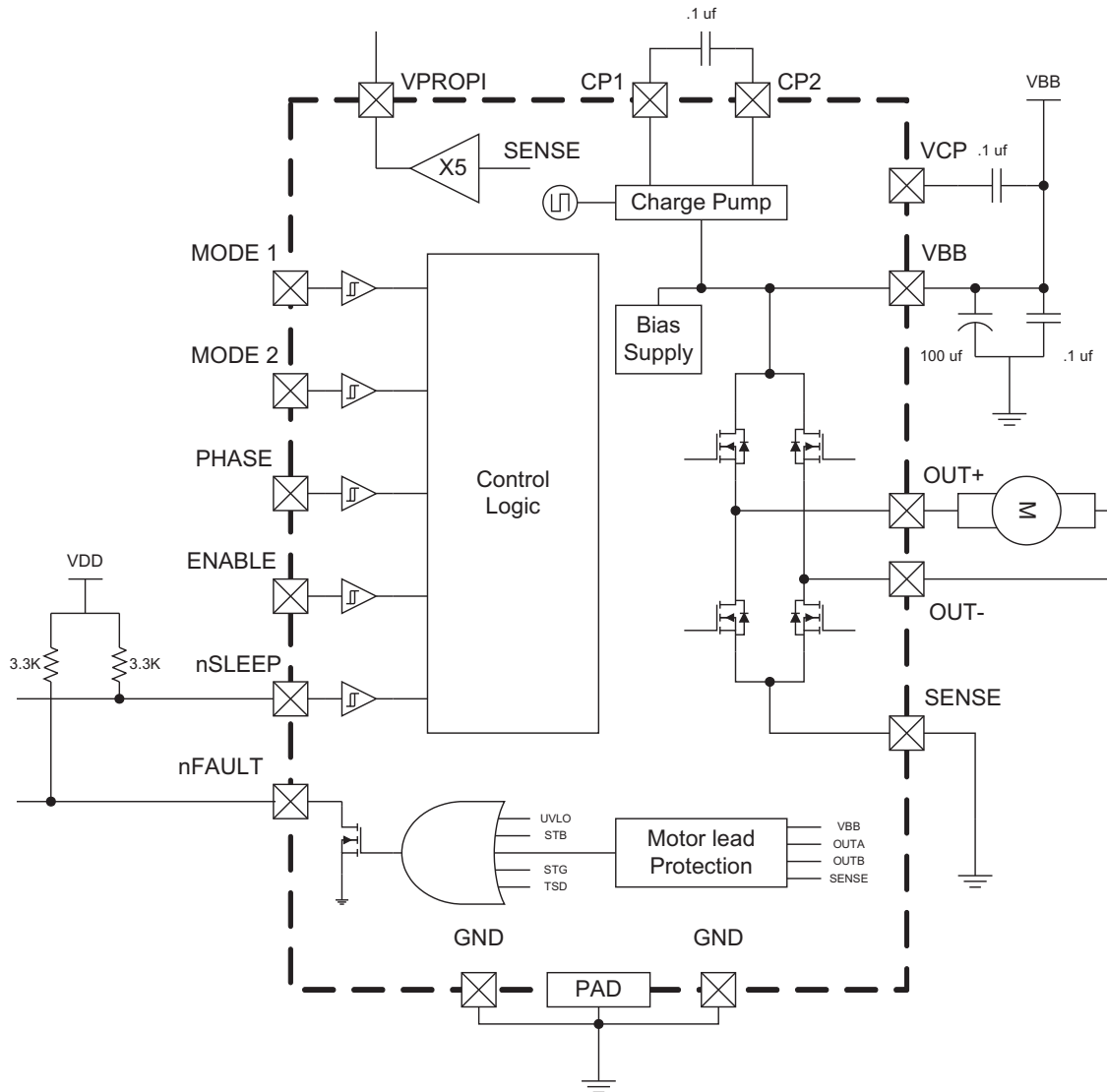
## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| VBB | Load supply voltage[2] |  | 40 | V |
|  | Output current |  | 2.8 | A |
| V$_{Sense}$ | Sense voltage |  | ±500 | mV |
|  | VBB to OUTx |  | 36 | V |
|  | OUTx to SENSE |  | 36 | V |
| VDD | Logic input voltage[2] | −0.3 | 7 | V |
| ESD rating | Human-Body Model (HBM) |  | ±2 | kV |
|  | Charged-Device Model (CDM) |  | 500 | V |
|  | Continuous total power dissipation | See Dissipation Rating Table |  |  |
| T$_A$ | Operating free-air temperature range | −20 | 80 | °C |
| T$_J$ | Maximum junction temperature |  | 190 | °C |
| T$_{stg}$ | Storage temperature range | −40 | 125 | °C |

(1)   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings
       only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating
       conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   All voltage values are with respect to network ground terminal.

## DISSIPATION RATINGS

| PACKAGE | θ$_{JA}$ | T$_A$ = 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T$_A$ = 25°C |
|---|---|---|---|
| RTY | 41.6 | 3 W | 24 mW/C |

## RECOMMENDED OPERATING CONDITIONS

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| V$_{IN}$ | Input voltage, VBB | 8 | 32 | 38 | V |
| T$_A$ | Operating free-air temperature | −20 | 25 | 80 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| IBB | Motor supply current | $f_{PWM}$ < 50 kHz | | 6 | | mA |
| | | Charge pump on, Outputs disabled | | 3.2 | | |
| | | Sleep mode | | | 10 | µA |
| $V_{IH}$ | PHASE, ENABLE, MODE input voltage | | 2 | | | V |
| $V_{IL}$ | | | | | 0.8 | |
| $V_{IH}$ | nSLEEP input voltage | | 2.7 | | | V |
| $V_{IL}$ | | | | | 0.8 | |
| $I_{IH}$ | PHASE, MODE input current 1 | $V_{IN}$ = 2 V | | <1.0 | 20 | µA |
| $I_{IL}$ | | $V_{IN}$ = 0.8 V | −20 | ≤−2.0 | 20 | |
| $I_{IH}$ | ENABLE input current | $V_{IN}$ = 2 V | | 40 | 100 | µA |
| $I_{IL}$ | | $V_{IN}$ = 0.8 V | | 16 | 40 | |
| $I_{IH}$ | nSLEEP input current | $V_{IN}$ = 2.7 V | | 27 | 50 | µA |
| $I_{IL}$ | | $V_{IN}$ = 0.8 V | | <1 | 10 | |
| $V_{OL}$ | nFAULT output voltage | $I_{sink}$ = 1 mA | | | 0.4 | V |
| VBBNFR | VBB nFAULT release | 8 V < VBB < 40 V | | 12 | 13.8 | V |
| $V_{IHys}$ | Input hysteresis, except nSLEEP | | 100 | 500 | 800 | mV |
| $R_{ds(ON)}$ | Output ON resistance | Source driver, $I_{OUT}$ = −2.8 A, $T_J$ = 25°C | | 0.35 | 0.48 | Ω |
| | | Source driver, $I_{OUT}$ = −2.8 A, $T_J$ = 125°C | | 0.55 | 0.8 | |
| | | Sink driver, $I_{OUT}$ = 2.8 A, $T_J$ = 25°C | | 0.3 | 0.43 | |
| | | Sink driver, $I_{OUT}$ = 2.8 A, $T_J$ = 125°C | | 0.45 | 0.7 | |
| VTRP | RSENSE/ISense voltage trip | SENSE connected to ground through some resistance | | 500 | | mV |
| $V_f$ | Body diode forward voltage 1 | Source diode, $I_f$ = −2.8 A | | | 1.4 | V |
| | | Sink diode, $I_f$ = 2.8 A | | | 1.4 | |
| $t_{pd}$ | Propagation delay time | PWM, Change to source or sink ON | | 600 | | ns |
| | | PWM, Change to source or sink OFF | | 100 | | |
| $t_{COD}$ | Crossover delay | | | 500 | | ns |
| DAGain | Differential AMP gain | Sense = 0.1 V to 0.4 V | | 5 | | V/V |
| **Protection Circuitry** | | | | | | |
| VUV | UVLO threshold | VBB increasing | | 6.5 | 8 | V |
| IOCP | Overcurrent threshold 2 | | 3 | | | A |
| $t_{OCP}$ | Overcurrent protection period | | | 1.2 | | ms |
| TJW | Thermal warning temperature | Temperature increasing | | 160 | | °C |
| TJWHys | Thermal warning hysteresis | Recovery = TJW – TJWHys | | 15 | | °C |
| TJTSD | Thermal shutdown temperature | Temperature increasing | | 175 | | °C |
| TJTSDHys | Thermal shutdown hysteresis | Recovery = TJTSD – TJTSDHys | | 15 | | °C |
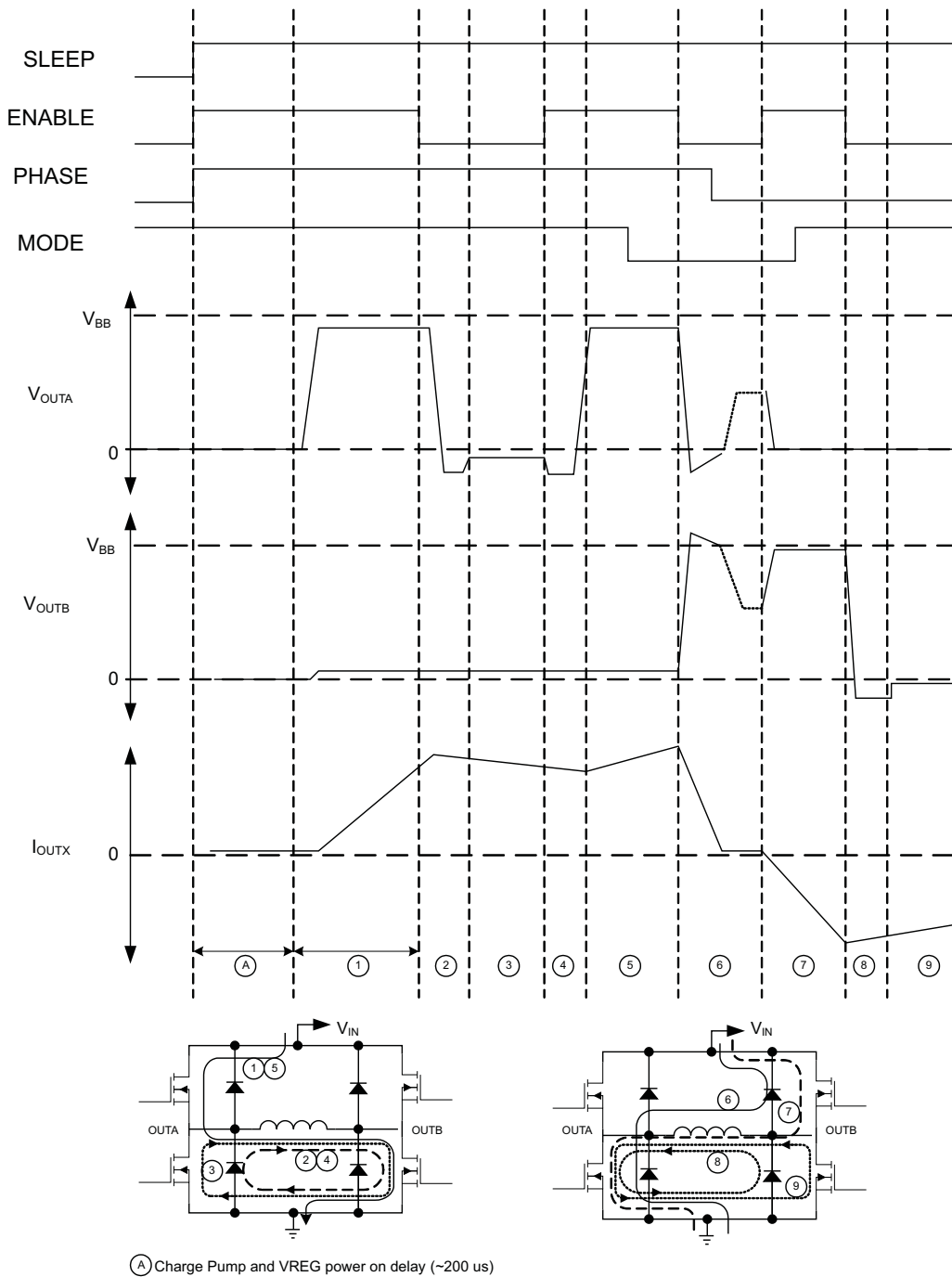
**Figure 1. PWM Control Timing**
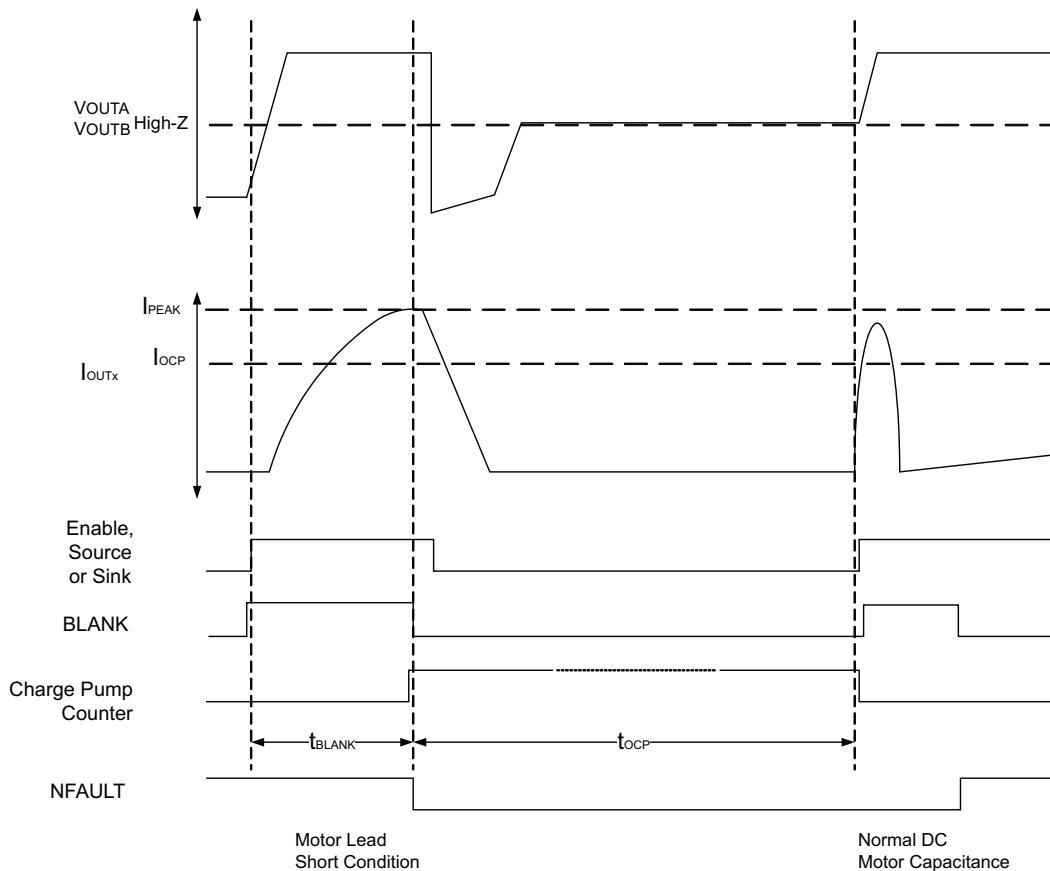
**Figure 2. Overcurrent Control Timing**

## FUNCTIONAL DESCRIPTION

### Device Operation

The DRV8800/DRV8801 is designed to drive one dc motor. The current through the output full-bridge switches and all N-channel DMOS are regulated with a fixed off-time PWM control circuit.

### Logic Inputs

It is recommended to use a high-value pullup resistor when logic inputs are pulled up to $V_{DD}$. This resistor limits the current to the input in case an overvoltage event occurs. Logic inputs are nSLEEP, MODE, PHASE, and ENABLE. Voltages higher than 7 V on any logic input can cause damage to the input structure.

### VREG (DRV8800 Only)

This output represents a measurement of the internal regulator voltage. This pin should be left disconnected. A voltage of approximately 7.5 V can be measured at this pin.

### VPROPI (DRV8801 Only)

This output offers an analog voltage proportional to the winding current. Voltage at this terminal is five times greater than the motor winding current (VPROPI = 5×I). VPROPI is meaningful only if there is a resistor connected to the SENSE pin. If SENSE is connected to ground, VPROPI measures 0 V. During slow decay, VPROPI outputs 0 V. VPROPI can output a maximum of 2.5 V, since at 500 mV on SENSE, the H-bridge is disabled.

## Charge Pump

The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1-µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1-µF ceramic monolithic capacitor, CStorage, should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

## Shutdown

As a measure to protect the device, faults caused by very high junction temperatures or low voltage on VCP disable the outputs of the device until the fault condition is removed. At power on, the UVLO circuit disables the drivers.

## Low-Power Mode

Control input nSLEEP is used to minimize power consumption when the DRV8800/DRV8801 is not in use. This disables much of the internal circuitry, including the internal voltage rails and charge pump. nSLEEP is asserted low. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

- MODE 1 (MODE on the DRV8800)

  Input MODE 1 is used to toggle between fast-decay mode and slow-decay mode. A logic high puts the device in slow-decay mode.

- MODE 2 (DRV8801 only)

  MODE 2 is used to select which set of drivers (high side versus low side) is used during the slow-decay recirculation. MODE 2 is meaningful only when MODE 1 is asserted high. A logic high on MODE 2 has current recirculation through the high-side drivers. A logic low has current recirculation through the low-side drivers.

## Braking

The braking function is implemented by driving the device in slow-decay mode (MODE 1 pin is high) and deasserting the enable to low. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor-generated BEMF as long as the ENABLE chop mode is asserted. The maximum current can be approximated by VBEMF/RL. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worse-case braking situations – high-speed and high-inertia loads.

## Diagnostic Output

The nFAULT pin signals a problem with the chip via an open-drain output. A motor fault, undervoltage condition, or $T_J > 160°C$ drives the pin active low. This output is not valid when nSLEEP puts the device into minimum power dissipation mode (i.e., nSLEEP is low). nFAULT stays asserted (nFAULT = L) until VBB reaches VBBNFR to give the charge pump headroom to reach its undervoltage threshold. nFAULT is a status-only signal and does not affect any device functionality. The H-bridge portion still operates normally down to VBB = 8 V with nFAULT asserted.

## Thermal Shutdown (TSD)

Two die-temperature monitors are integrated on the chip. As die temperature increases toward the maximum, a thermal warning signal is triggered at 160°C. This fault drives the nFAULT low, but does not disable the operation of the chip. If the die temperature increases further, to approximately 175°C, the full-bridge outputs are disabled until the internal temperature falls below a hysteresis of 15°C.

### Control Logic Table[1]

| PINS | | | | | | | OPERATION |
|---|---|---|---|---|---|---|---|
| PHASE | ENABLE | MODE 1 | MODE 2 | nSLEEP | OUTA | OUTB | |
| 1 | 1 | X | X | 1 | H | L | Forward |
| 0 | 1 | X | X | 1 | L | H | Reverse |
| X | 0 | 1 | 0 | 1 | L | L | Brake (slow decay) |
| 1 | 0 | 0 | 1 | 1 | L | H | Fast-decay synchronous rectification[2] |
| 0 | 0 | 0 | X | 1 | H | L | Fast-decay synchronous rectification[2] |
| X | X | X | X | 0 | Z | Z | Sleep mode |

(1)    X = Don't care, Z = high impedance
(2)    To prevent reversal of current during fast-decay synchronous rectification, outputs go to the high-impedance state as the current
        approaches 0 A.

## Overcurrent Protection

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, the full-bridge outputs are turned off, flag nFAULT is driven low, and a 1.2-ms fault timer is started. After this 1.2-ms period, $t_{OCP}$, the device is then allowed to follow the input commands and another turnon is attempted (nFAULT becomes high again during this attempt). If there is still a fault condition, the cycle repeats. If after $t_{OCP}$ expires it is determined the short condition is not present, normal operation resumes and nFAULT is deasserted.

## APPLICATION INFORMATION

### Power Dissipation

First-order approximation of power dissipation in the DRV8800/DRV8801 can be calculated by examining the power dissipation in the full-bridge during each of the operation modes. DRV8800/DRV8801 utilize synchronous rectification. During the decay cycle, the body diode is shorted by the low-$R_{ds(ON)}$ driver, which in turn reduces power dissipation in the full-bridge. In order to prevent shoot through (high-side and low-side drivers on the same side are ON at the same time), DRV8800/DRV8801 implement a 500-ns typical crossover delay time. During this period, the body diode in the decay current path conducts the current until the DMOS driver turns on. High current and high ambient temperature applications should take this into consideration. In addition, motor parameters and switching losses can add power dissipation that could affect critical applications.

### Drive Current

This current path is through the high-side sourcing DMOS driver, motor winding, and low-side sinking DMOS driver. Power dissipation I2R loses in one source and one sink DMOS driver, as shown in Equation 1.

$$P_D = I^2(R_{DS(on)Source} + R_{DS(onSink)})$$

(1)

DRV8800
DRV8801

TEXAS
INSTRUMENTS

SLVS855A−JULY 2008−REVISED JULY 2008

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**DRV8800**



1 Drive Current
2 Fast decay with synchronous rectification (reverse)
3 Slow decay with synchronous rectification (brake)

**DRV8801**



1 Drive Current
2 Fast decay with synchronous rectification (reverse)
3 Slow decay with synchronous rectification (brake) Low Side
4 Slow decay with synchronous rectification (brake) High Side

**Figure 3. Current Path**

## Fast Decay With Synchronous Rectification

This decay mode is equivalent to a phase change where the opposite drivers are switched on. When in fast decay, the motor current is not allowed to go negative (direction change). Instead, as the current approaches zero, the drivers turn off. The power calculation is the same as the drive current calculation (see Equation 1).

## Slow-Decay SR (Brake Mode)

In slow-decay mode, both low-side sinking drivers turn on, allowing the current to circulate through the H-bridge's low side (two sink drivers) and the load. Power dissipation I2R loses in the two sink DMOS drivers:

$$P_D = I^2(2 \times R_{DS(on)Sink})$$

(2)

## SENSE

A low-value resistor can be placed between the SENSE pin and ground for current-sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current-sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

**NOTE:**

When selecting a value for the sense resistor, SENSE does not exceed the maximum voltage of ±500 mV. The H-bridge is disabled and enters recirculation while motor winding current is above a SENSE voltage equal or greater than 500 mV.

## Ground

A ground power plane should be located as close to the DRV8800/DRV8801 as possible. The copper ground plane directly under the PowerPAD package makes a good location. This pad can then be connected to ground for this purpose.

## Layout

The printed circuit board (PCB) should use a heavy ground plane. For optimum electrical and thermal performance, the DRV8800/DRV8801 must be soldered directly onto the board. On the underside of the DRV8800/DRV8801 is a PowerPAD package, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB. For more information on this technique, please refer to document SLMA002.

The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 μF) in parallel with a ceramic capacitor placed as close as possible to the device. The ceramic capacitors between VCP and VBB, connected to VREG, and between CP1 and CP2 should be as close to the pins of the device as possible, in order to minimize lead inductance.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| DRV8800RTYR | ACTIVE | QFN | RTY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| DRV8800RTYT | ACTIVE | QFN | RTY | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| DRV8801RTYR | ACTIVE | QFN | RTY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| DRV8801RTYT | ACTIVE | QFN | RTY | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

**[1]** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**[2]** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**[3]** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV8800RTYR | QFN | RTY | 16 | 3000 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| DRV8800RTYT | QFN | RTY | 16 | 250 | 180.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| DRV8801RTYR | QFN | RTY | 16 | 3000 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| DRV8801RTYT | QFN | RTY | 16 | 250 | 180.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

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**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| DRV8800RTYR | QFN | RTY | 16 | 3000 | 346.0 | 346.0 | 29.0 |
| DRV8800RTYT | QFN | RTY | 16 | 250 | 190.5 | 212.7 | 31.8 |
| DRV8801RTYR | QFN | RTY | 16 | 3000 | 346.0 | 346.0 | 29.0 |
| DRV8801RTYT | QFN | RTY | 16 | 250 | 190.5 | 212.7 | 31.8 |

## RTY (S−PQFP−N16)                                PLASTIC QUAD FLATPACK

$\frac{4,15}{3,85}$

$\frac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{0,80}{0,70}$

0,20 REF.

SEATING PLANE

⌷ 0,08

$\frac{0,05}{0,00}$

16X $\frac{0,65}{0,45}$

0,65

1    4

16    5

13    8

EXPOSED THERMAL PAD ⟨D⟩

12    9

1,95

16X $\frac{0,38}{0,23}$

⊕ ⌀ 0,10 Ⓜ
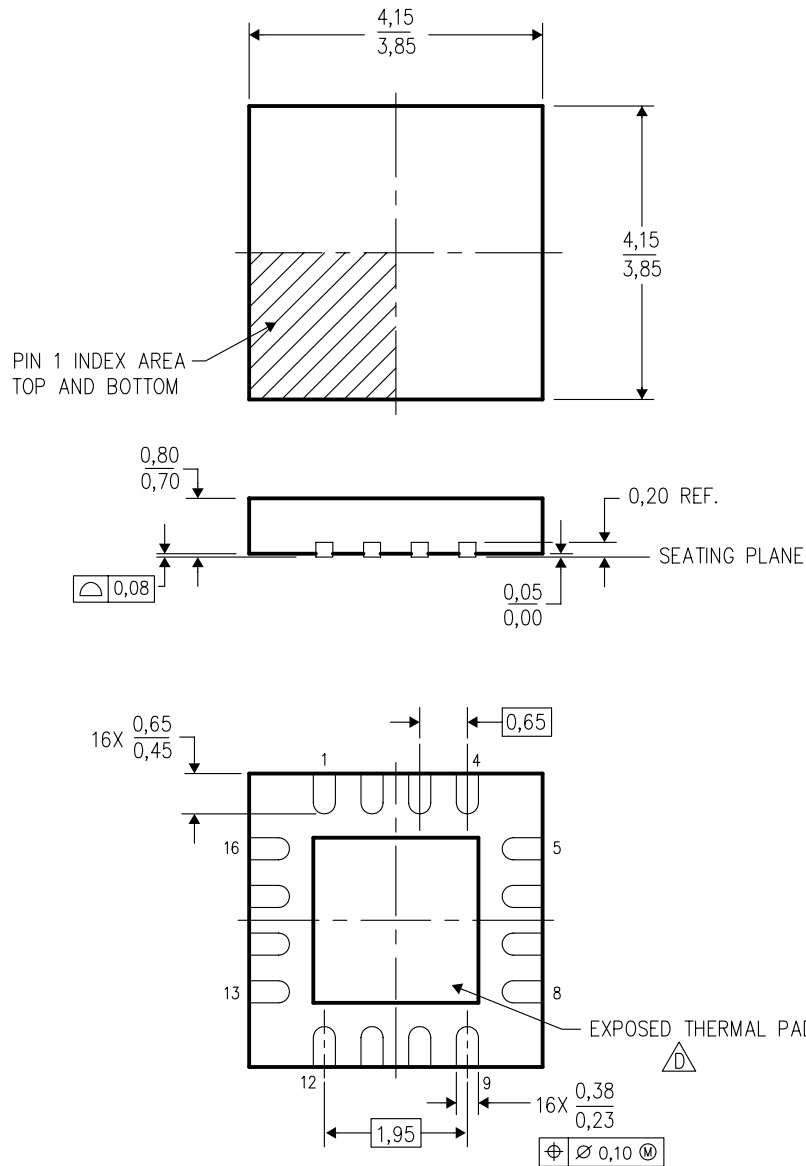
4206276/A   08/04

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−leads (QFN) package configuration.
     ⟨D⟩  The package thermal pad must be soldered to the board for thermal and mechanical performance.
              See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
         E.   Falls within JEDEC MO−220.