74LVC4245A

Octal dual supply translating transceiver; 3-state

Rev. 10 — 18 December 2012 — Product data sheet

1. General description

The 74LVC4245A is an octal dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

The device features an output enable input (pin $\overline{OE}$) for easy cascading and a send/receive input (pin DIR) for direction control. Pin $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

In suspend mode, when $V_{CC(A)}$ is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-state and the voltage on the A-bus must be smaller than V_{diode} (typical 0.7 V).

$V_{CC(A)} \geq V_{CC(B)}$, except in suspend mode.

2. Features and benefits

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range:
  - 3 V bus ($V_{CC(B)}$): 1.5 V to 3.6 V
  - 5 V bus ($V_{CC(A)}$): 1.5 V to 5.5 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when $V_{CC(A)}$ = 0 V
- Complies with JEDEC standard no. JESD8B/JESD36
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC4245AD	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC4245ADB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC4245APW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74LVC4245ABQ	–40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

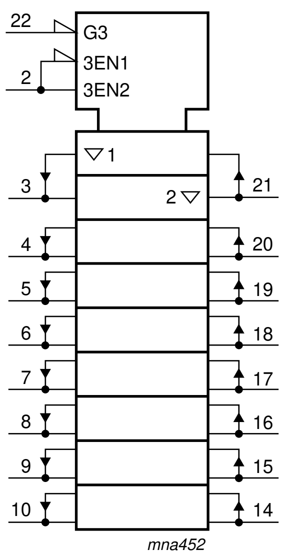


Fig 1. IEC Logic symbol

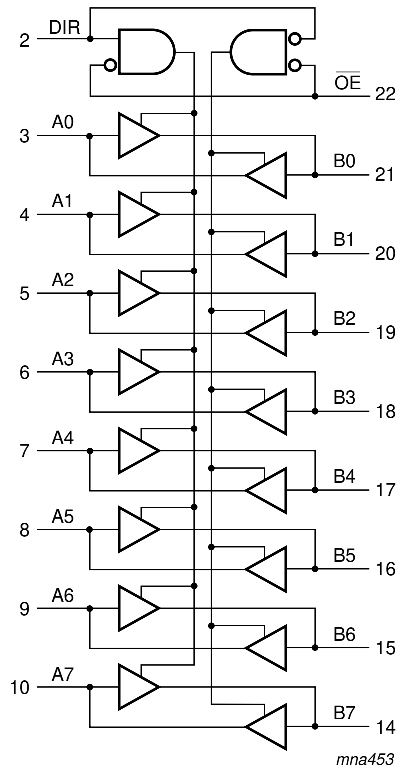


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

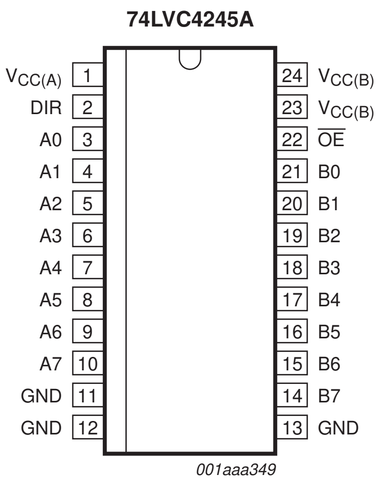
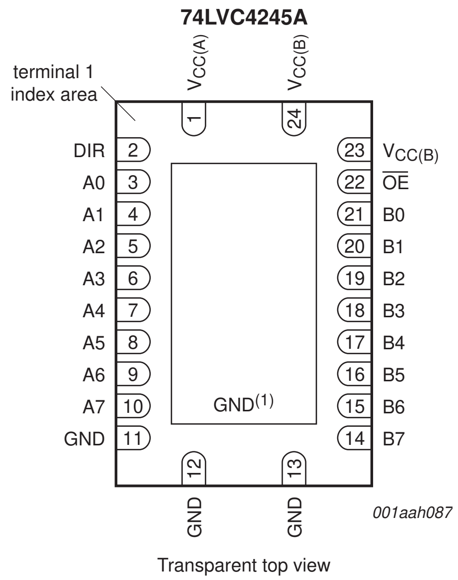


Fig 3. Pin configuration SO24 and (T)SSOP24



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 4. Pin configuration DHVQFN24

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage (5 V bus)
$V_{CC(B)}$	23, 24	supply voltage (3 V bus)
GND	11, 12, 13	ground (0 V)
DIR	2	direction control
A[0:7]	3, 4, 5, 6, 7, 8, 9, 10	data input or output
B[0:7]	21, 20, 19, 18, 17, 16, 15, 14	data input or output
$\overline{OE}$	22	output enable input (active LOW)

6. Functional description

Table 3. Functional table[1]

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			–0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CCO}$ or $V_O < 0$ V	[3]	-	±50	mA
V_O	output voltage	output HIGH or LOW state	[1]	–0.5	V_{CC} + 0.5	V
		output 3-state	[1]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CCO}	[3]	-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN24 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

[3] V_{CCO} is the supply voltage associated with the output.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(A)}$	supply voltage A	$V_{CC(A)} \geq V_{CC(B)}$; see Figure 5 for maximum speed performance	1.5	-	5.5	V
$V_{CC(B)}$	supply voltage B	$V_{CC(A)} \geq V_{CC(B)}$; see Figure 5 for low-voltage applications	1.5	-	3.6	V
V_I	input voltage	for control inputs	0	-	5.5	V

Table 5. Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature		–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC(B)}$ = 2.7 V to 3.0 V	-	-	20	ns/V
		$V_{CC(B)}$ = 3.0 V to 3.6 V	-	-	10	ns/V
		$V_{CC(A)}$ = 3.0 V to 4.5 V	-	-	20	ns/V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V	2.0	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V	-	-	0.8	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = –100 μA	$V_{CC(B)}$ – 0.2	$V_{CC(B)}$	-	V
		$V_{CC(B)}$ = 2.7 V; I_O = –12 mA	$V_{CC(B)}$ – 0.5	-	-	V
		$V_{CC(B)}$ = 3.0 V; I_O = –24 mA	$V_{CC(B)}$ – 0.8	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = –100 μA	$V_{CC(A)}$ – 0.2	$V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = –12 mA	$V_{CC(A)}$ – 0.5	-	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = –24 mA	$V_{CC(A)}$ – 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = 100 μA	-	-	0.20	V
		$V_{CC(B)}$ = 2.7 V; I_O = 12 mA	-	-	0.40	V
		$V_{CC(B)}$ = 3.0 V; I_O = 24 mA	-	-	0.55	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = 100 μA	-	-	0.20	V
		$V_{CC(A)}$ = 4.5 V; I_O = 12 mA	-	-	0.40	V
		$V_{CC(A)}$ = 4.5 V; I_O = 24 mA	-	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND	-	±0.1	±5	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} [2]				
		$V_{CC(B)}$ = 3.6 V; V_O = $V_{CC(B)}$ or GND	-	±0.1	±5	μA
		$V_{CC(A)}$ = 5.5 V; V_O = $V_{CC(A)}$ or GND	-	±0.1	±5	μA
I_{CC}	supply current	I_O = 0 A				
		$V_{CC(B)}$ = 3.6 V; other inputs at $V_{CC(B)}$ or GND	-	0.1	10	μA
		$V_{CC(A)}$ = 5.5 V; other inputs at $V_{CC(A)}$ or GND	-	0.1	10	μA

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ΔI_{CC}	additional supply current	per control pin; I_O = 0 A	[3]				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; $V_I = V_{CC(B)} - 0.6$ V; other inputs at $V_{CC(B)}$ or GND		-	5	500	μA
		$V_{CC(A)}$ = 4.5 V to 5.5 V; $V_I = V_{CC(A)} - 0.6$ V; other inputs at $V_{CC(A)}$ or GND		-	5	500	μA
C_I	input capacitance			-	4.0	-	pF
$C_{I/O}$	input/output capacitance	An and Bn		-	5.0	-	pF
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V		2.0	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V		-	-	0.8	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = −100 μA		$V_{CC(B)} - 0.3$	-	-	V
		$V_{CC(B)}$ = 2.7 V; I_O = −12 mA		$V_{CC(B)} - 0.65$	-	-	V
		$V_{CC(B)}$ = 3.0 V; I_O = −24 mA		$V_{CC(B)} - 1.0$	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = −100 μA		$V_{CC(A)} - 0.3$	-	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = −12 mA		$V_{CC(A)} - 0.65$	-	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = −24 mA		$V_{CC(A)} - 1.0$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = 100 μA		-	-	0.30	V
		$V_{CC(B)}$ = 2.7 V; I_O = 12 mA		-	-	0.60	V
		$V_{CC(B)}$ = 3.0 V; I_O = 24 mA		-	-	0.80	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = 100 μA		-	-	0.30	V
		$V_{CC(A)}$ = 4.5 V; I_O = 12 mA		-	-	0.60	V
		$V_{CC(A)}$ = 4.5 V; I_O = 24 mA		-	-	0.80	V
I_I	input leakage current	V_I = 5.5 V or GND		-	-	±20	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}	[2]				
		$V_{CC(B)}$ = 3.6 V; $V_O = V_{CC(B)}$ or GND		-	-	±20	μA
		$V_{CC(A)}$ = 5.5 V; $V_O = V_{CC(A)}$ or GND		-	-	±20	μA
I_{CC}	supply current	I_O = 0 A					
		$V_{CC(B)}$ = 3.6 V; other inputs at $V_{CC(B)}$ or GND		-	-	40	μA
		$V_{CC(A)}$ = 5.5 V; other inputs at $V_{CC(A)}$ or GND		-	-	40	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ΔI_{CC}	additional supply current	per control pin; I_O = 0 A	[3]				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; $V_I = V_{CC(B)} - 0.6$ V; other inputs at $V_{CC(B)}$ or GND		-	-	5000	μA
		$V_{CC(A)}$ = 4.5 V to 5.5 V; $V_I = V_{CC(A)} - 0.6$ V; other inputs at $V_{CC(A)}$ or GND		-	-	5000	μA

[1] All typical values are measured at $V_{CC(A)}$ = 5.0 V, $V_{CC(B)}$ = 3.3 V and T_{amb} = 25 °C.

[2] For transceivers, the parameter I_{OZ} includes the input leakage current.

[3] $V_{CC(B)}$ = 2.7 V to 3.6 V: other inputs at $V_{CC(B)}$ or GND.
$V_{CC(A)}$ = 4.5 V to 5.5 V: other inputs at $V_{CC(A)}$ or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). $V_{CC(A)}$ = 4.5 V to 5.5 V; $t_r = t_f \leq 2.5$ ns. For test circuit see Figure 8.

Symbol	Parameter	Conditions	$V_{CC(B)}$	–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	An to Bn; see Figure 6	2.7 V	1.0	3.6	6.3	1.0	8.0	ns
			3.0 V to 3.6 V	1.0	3.3	6.3	1.0	8.0	ns
		Bn to An; see Figure 6	2.7 V	1.0	3.4	6.1	1.0	8.0	ns
			3.0 V to 3.6 V	1.0	3.4	6.1	1.0	8.0	ns
t_{PLH}	LOW to HIGH propagation delay	An to Bn; see Figure 6	2.7 V	1.0	3.3	6.7	1.0	8.5	ns
			3.0 V to 3.6 V	1.0	2.8	6.5	1.0	8.5	ns
		Bn to An; see Figure 6	2.7 V	1.0	3.0	5.0	1.0	6.5	ns
			3.0 V to 3.6 V	1.0	3.0	5.0	1.0	6.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to An; see Figure 7	2.7 V	1.0	4.5	9.0	1.0	11.5	ns
			3.0 V to 3.6 V	1.0	4.5	9.0	1.0	11.5	ns
		$\overline{OE}$ to Bn; see Figure 7	2.7 V	1.0	4.4	8.7	1.0	11.0	ns
			3.0 V to 3.6 V	1.0	3.8	8.1	1.0	10.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to An; see Figure 7	2.7 V	1.0	4.5	8.1	1.0	10.5	ns
			3.0 V to 3.6 V	1.0	4.5	8.1	1.0	10.5	ns
		$\overline{OE}$ to Bn; see Figure 7	2.7 V	1.0	4.3	8.7	1.0	11.0	ns
			3.0 V to 3.6 V	1.0	3.2	8.1	1.0	10.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to An; see Figure 7	2.7 V	1.0	2.9	7.0	1.0	9.0	ns
			3.0 V to 3.6 V	1.0	2.9	7.0	1.0	9.0	ns
		$\overline{OE}$ to Bn; see Figure 7	2.7 V	1.0	3.9	7.7	1.0	10.0	ns
			3.0 V to 3.6 V	1.0	3.5	7.7	1.0	10.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to An; see Figure 7	2.7 V	1.0	2.8	5.8	1.0	7.5	ns
			3.0 V to 3.6 V	1.0	2.8	5.8	1.0	7.5	ns
		$\overline{OE}$ to Bn; see Figure 7	2.7 V	1.0	3.3	7.8	1.0	10.0	ns
			3.0 V to 3.6 V	1.0	2.9	7.8	1.0	10.0	ns

Table 7. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V). $V_{CC(A)}$ = 4.5 V to 5.5 V; $t_r = t_f \leq 2.5$ ns. For test circuit see Figure 8.

Symbol	Parameter	Conditions	$V_{CC(B)}$	−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
$t_{sk(o)}$	output skew time		[2]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	5 V bus: Bn to An; V_I = GND to $V_{CC(A)}$; $V_{CC(A)}$ = 5.0 V	[3]						
		outputs enabled	-	-	17	-	-	-	pF
		outputs disabled	-	-	5	-	-	-	pF
		3 V bus: An to Bn; V_I = GND to $V_{CC(B)}$; $V_{CC(B)}$ = 3.3 V	[3]						
		outputs enabled	-	-	17	-	-	-	pF
		outputs disabled	-	-	5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C, $V_{CC(A)}$ = 5.0 V, and $V_{CC(B)}$ = 2.7 V and 3.3 V respectively.

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. AC waveforms

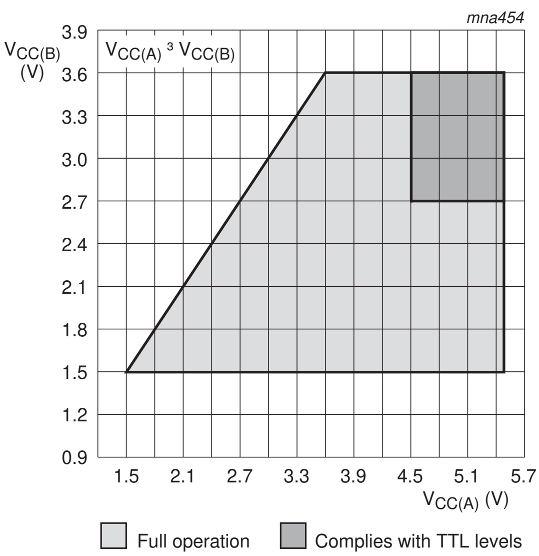
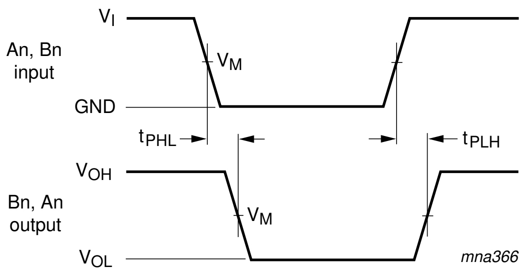


Fig 5. Supply operation area

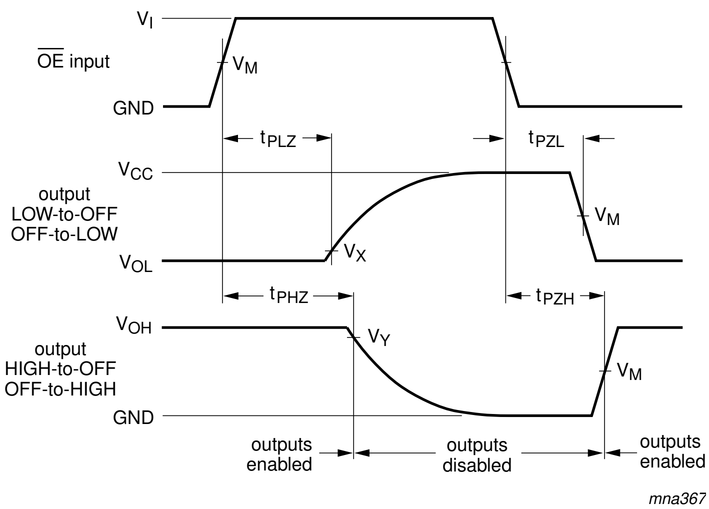


V_M = 1.5 V at 2.7 V ≤ $V_{CC(B)}$ ≤ 3.6 V;

V_M = 0.5 $V_{CC(A)}$ at $V_{CC(A)}$ ≥ 4.5 V.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 6. Input (An, Bn) to output (Bn, An) propagation delays



V_M = 1.5 V at 2.7 V ≤ $V_{CC(B)}$ ≤ 3.6 V;

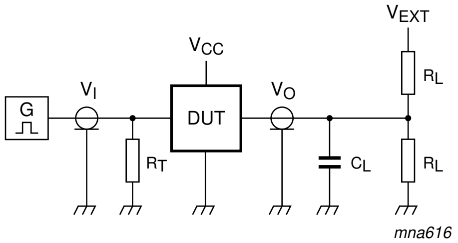
V_M = 0.5 $V_{CC(A)}$ at $V_{CC(A)}$ ≥ 4.5 V.

V_X = V_{OL} + 0.3 V at $V_{CC(B)}$ ≥ 2.7 V;

V_Y = V_{OH} − 0.3 V at $V_{CC(B)}$ ≥ 2.7 V.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 7. 3-state enable and disable times



Test data is given in Table 8. Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 8. Load circuitry for switching times

Table 8. Test data

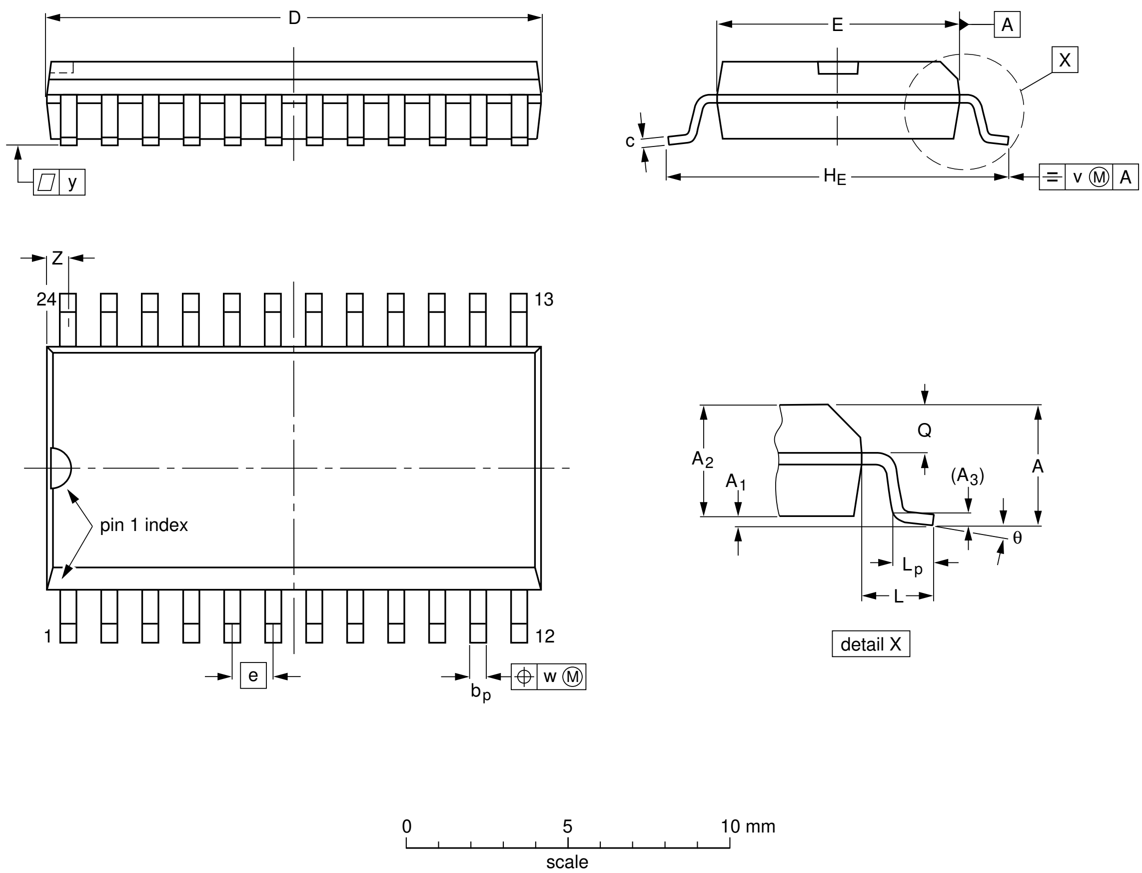
Supply voltage		Input	Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [2]
< 2.7 V	< 2.7 V	V_{CCI}	50 pF	500 Ω	open	GND	2 × V_{CCO}
-	2.7 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V_{CCO}
4.5 V to 5.5 V	-	3.0 V	50 pF	500 Ω	open	GND	2 × V_{CCO}

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

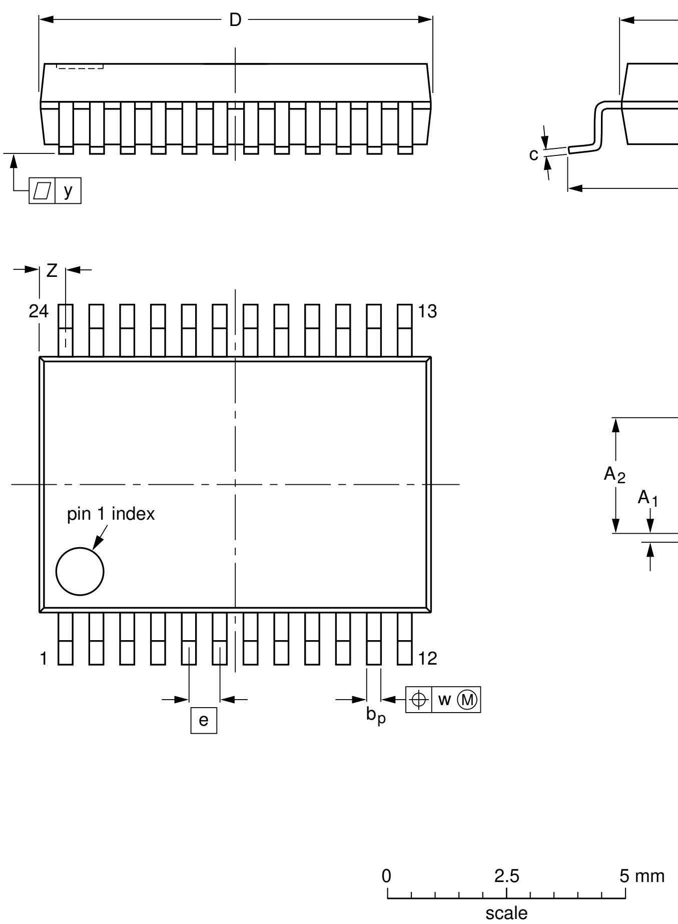
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

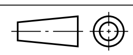
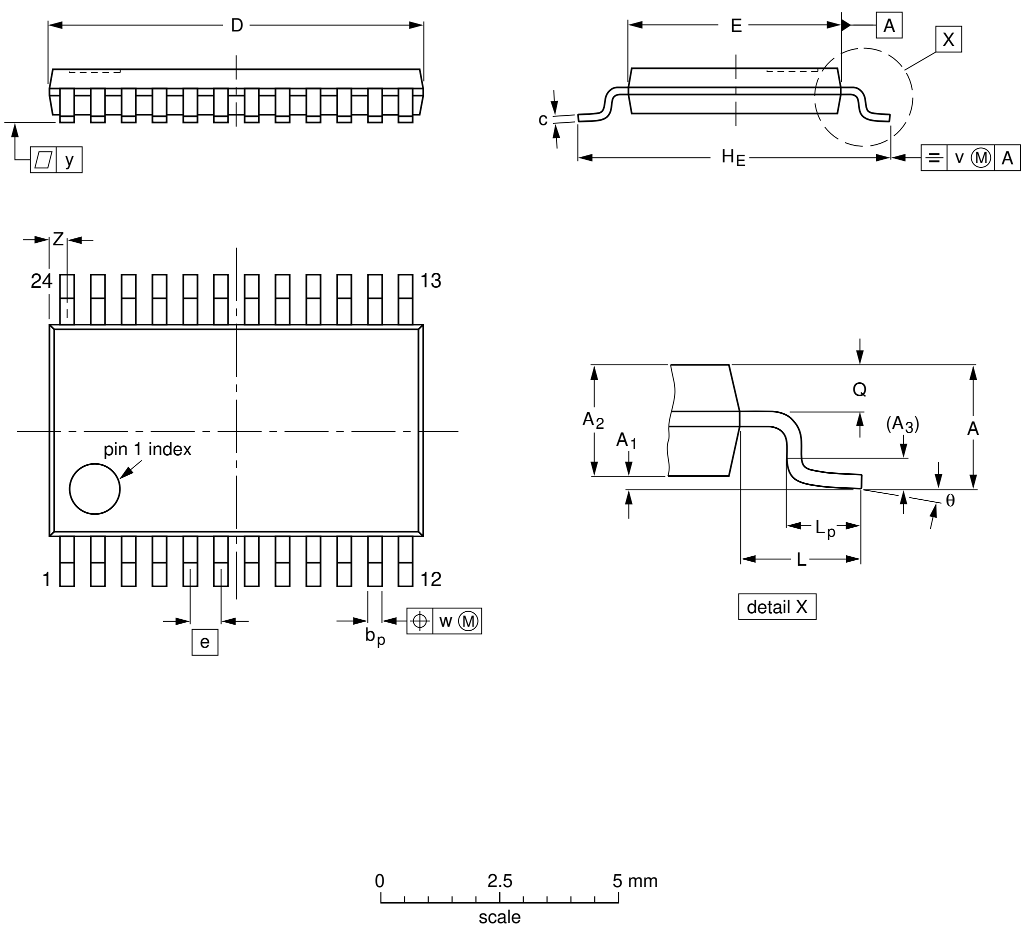
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

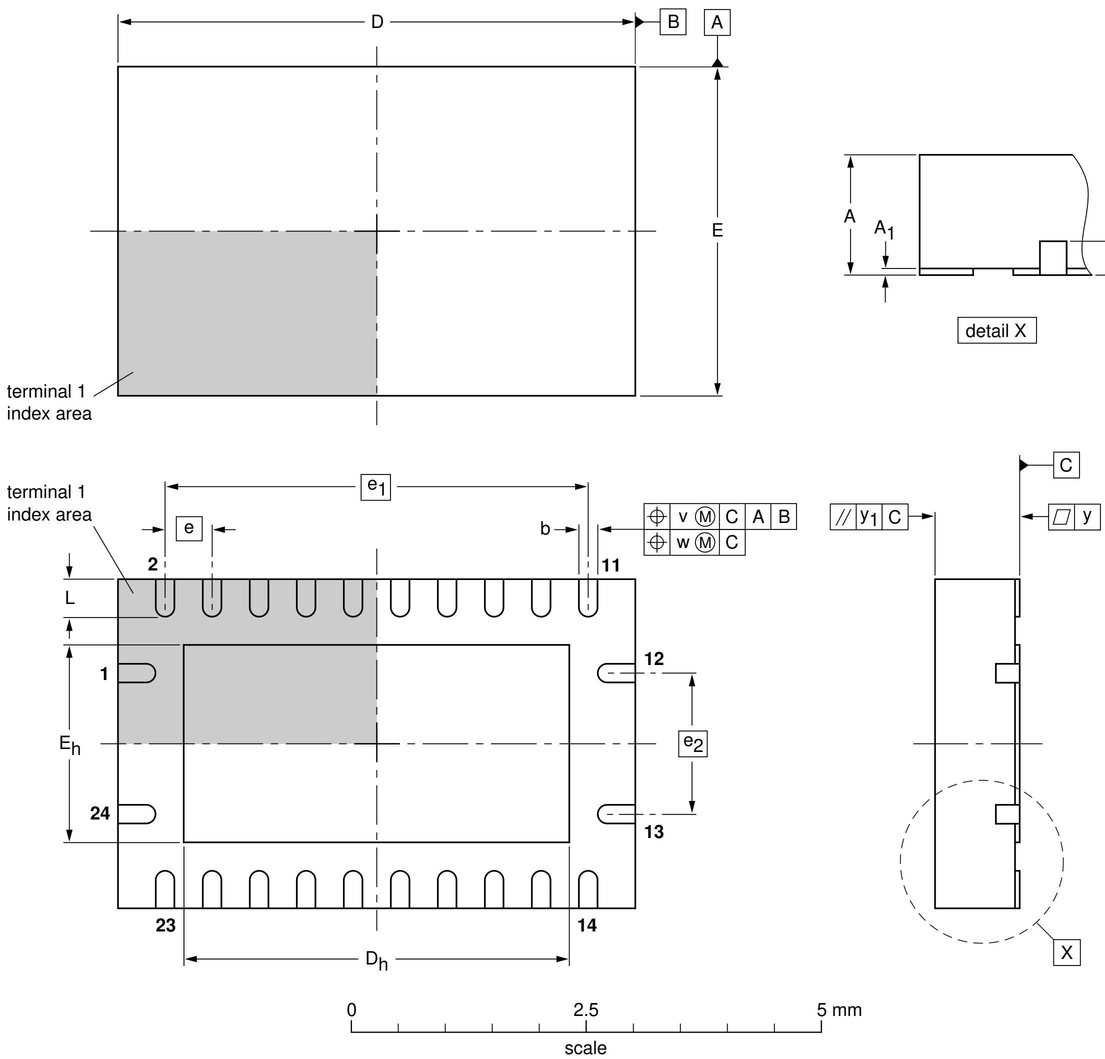
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig 12. Package outline SOT815-1 (DHVQFN24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC4245A v.10	20121218	Product data sheet	-	74LVC4245A v.9
Modifications:	• $V_{CC(A)}$ and $V_{CC(B)}$ changed into $V_{CC(A)}$ and $V_{CC(B)}$ (errata)			
74LVC4245A v.9	20121120	Product data sheet	-	74LVC4245A v.8
Modifications:	• Figure 4: Pin configuration drawing corrected for DHVQFN24 package			
74LVC4245A v.8	20111122	Product data sheet	-	74LVC4245A v.7
74LVC4245A v.7	20110812	Product data sheet	-	74LVC4245A v.6
74LVC4245A v.6	20080118	Product data sheet	-	74LVC4245A v.5
74LVC4245A v.5	20040330	Product specification	-	74LVC4245A v.4
74LVC4245A v.4	20040211	Product specification	-	74LVC4245A v.3
74LVC4245A v.3	19990615	Product specification	-	74LVC4245A v.2
74LVC4245A v.2	19980729	Product specification	-	74LVC4245A v.1
74LVC4245A v.1	19980729	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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