

Features

- Wide Range of Digital and Analog Signal Levels
 - Digital 3V to 20V
 - Analog $\leq 20V_{P-P}$
- Low ON Resistance, 125 Ω (Typ) Over 15V_{P-P} Signal Input Range for $V_{DD}-V_{EE} = 18V$
- High OFF Resistance, Channel Leakage of $\pm 100pA$ (Typ) at $V_{DD}-V_{EE} = 18V$
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V ($V_{DD}-V_{SS} = 3V$ to 20V) to Switch Analog Signals to 20V_{P-P} ($V_{DD}-V_{EE} = 20V$)
- Matched Switch Characteristics, $r_{ON} = 5\Omega$ (Typ) for $V_{DD}-V_{EE} = 15V$
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 μW (Typ) at $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V$
- Binary Address Decoding on Chip
- 5V, 10V, and 15V Parametric Ratings
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1 μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25 $^{\circ}C$
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V_{P-P} can be achieved by digital signal amplitudes of 4.5V to 20V (if $V_{DD}-V_{SS} = 3V$, a $V_{DD}-V_{EE}$ of up to 13V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13V, a $V_{DD}-V_{SS}$ of at least 4.5V is required). For example, if $V_{DD} = +4.5V$, $V_{SS} = 0V$, and $V_{EE} = -13.5V$, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

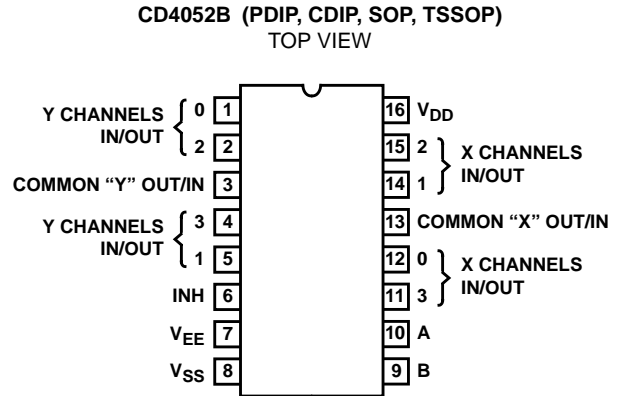
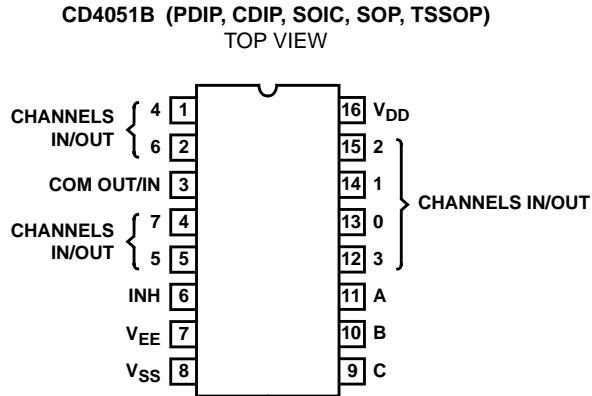
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4051BF3A, CD4052BF3A, CD4053BF3A	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BMT, CD4051BM96 CD4052BM, CD4052BMT, CD4052BM96 CD4053BM, CD4053BMT, CD4053BM96	-55 to 125	16 Ld SOIC
CD4051BNSR, CD4052BNSR, CD4053BNSR	-55 to 125	16 Ld SOP
CD4051BPW, CD4051BPWR, CD4052BPW, CD4052BPWR, CD4053BPW, CD4053BPWR	-55 to 125	16 Ld TSSOP

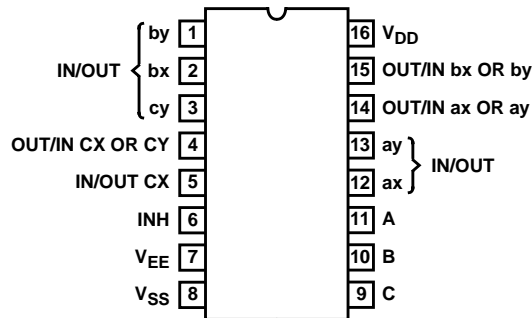
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CD4051B, CD4052B, CD4053B

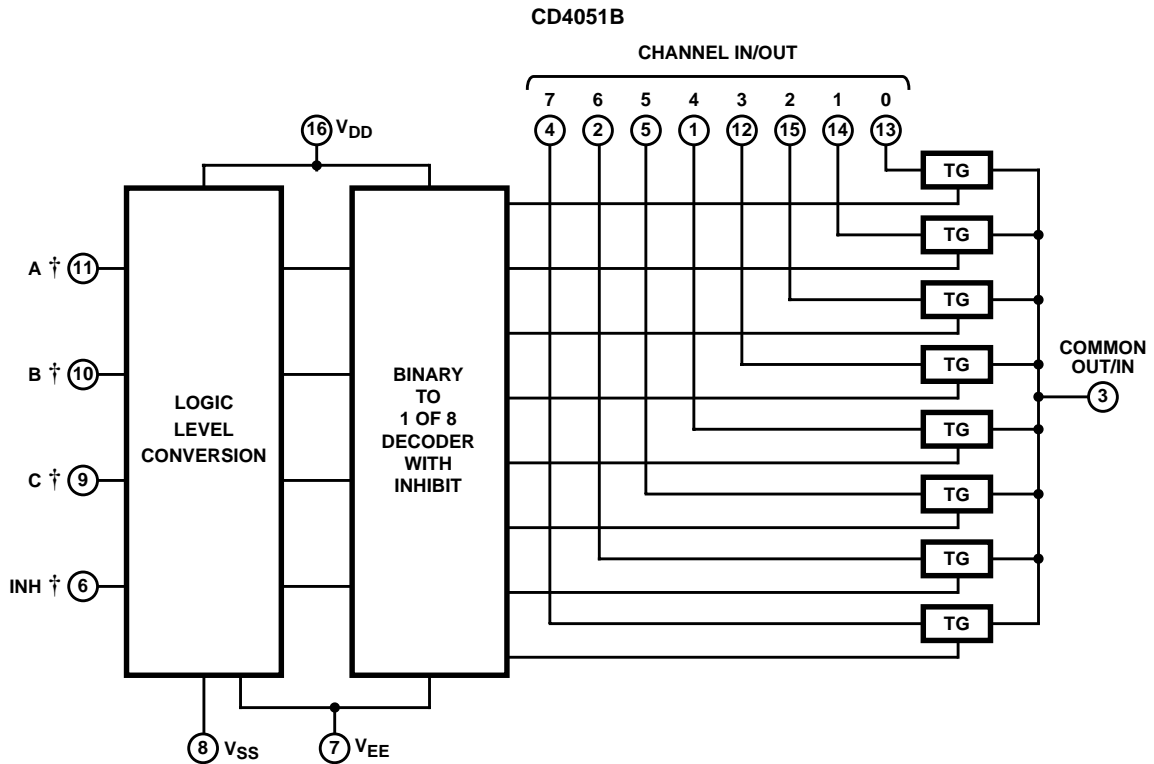
Pinouts



CD4053B (PDIP, CDIP, SOP, TSSOP)
TOP VIEW



Functional Block Diagrams

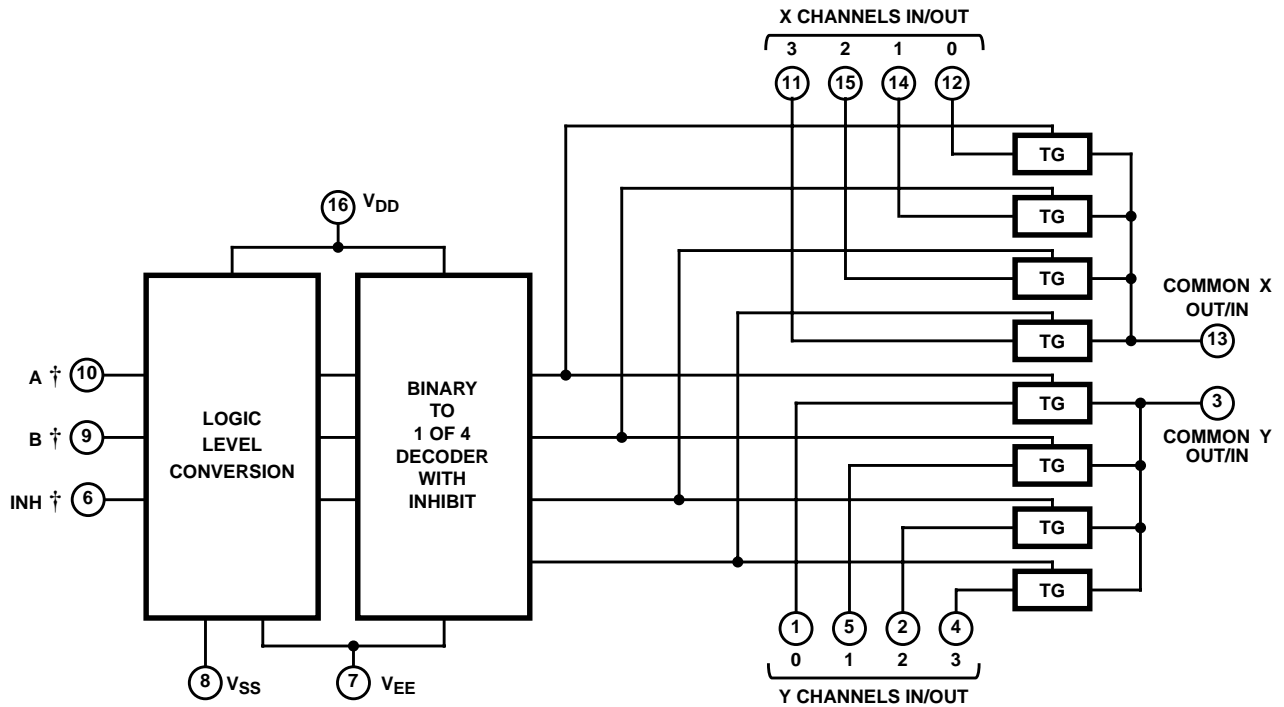


† All inputs are protected by standard CMOS protection network.

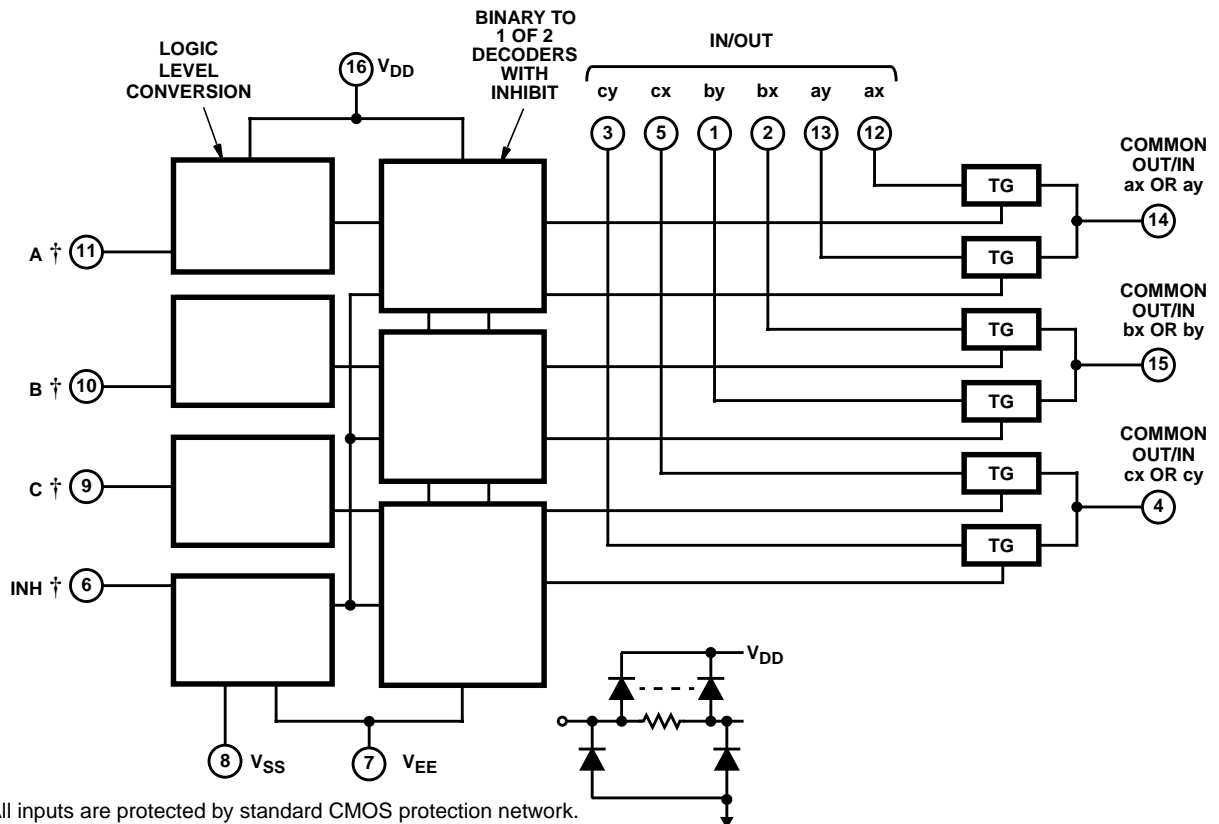
CD4051B, CD4052B, CD4053B

Functional Block Diagrams (Continued)

CD4052B



CD4053B



† All inputs are protected by standard CMOS protection network.

CD4051B, CD4052B, CD4053B

TRUTH TABLES

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
INHIBIT	B		A	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
CD4053B				
INHIBIT	A OR B OR C			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

X = Don't Care

CD4051B, CD4052B, CD4053B

Absolute Maximum Ratings

Supply Voltage (V+ to V-)

Voltages Referenced to V_{SS} Terminal -0.5V to 20V
 DC Input Voltage Range -0.5V to V_{DD} +0.5V
 DC Input Current, Any One Input. ±10mA

Operating Conditions

Temperature Range -55°C to 125°C

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):

E (PDIP) package. 67°C/W
 M (SOIC) package 73°C/W
 NS (SOP) package. 64°C/W
 PW (TSSOP) package 108°C/W
 Maximum Junction Temperature (Ceramic Package) 175°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range. -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 265°C
 (SOIC - Lead Tips Only)


CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Specifications

Common Conditions Here: If Whole Table is For the Full Temp. Range, V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS		
	V _{IS} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	-55	-40	85	125	25					
									MIN	TYP	MAX			
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})														
Quiescent Device Current, I _{DD} Max	-	-	-	5	5	5	150	150	-	0.04	5	μA		
	-	-	-	10	10	10	300	300	-	0.04	10	μA		
	-	-	-	15	20	20	600	600	-	0.04	20	μA		
	-	-	-	20	100	100	3000	3000	-	0.08	100	μA		
Drain to Source ON Resistance r _{ON} Max 0 ≤ V _{IS} ≤ V _{DD}	-	0	0	5	800	850	1200	1300	-	470	1050	Ω		
	-	0	0	10	310	330	520	550	-	180	400	Ω		
	-	0	0	15	200	210	300	320	-	125	240	Ω		
Change in ON Resistance (Between Any Two Channels), Δr _{ON}	-	0	0	5	-	-	-	-	-	15	-	Ω		
	-	0	0	10	-	-	-	-	-	10	-	Ω		
	-	0	0	15	-	-	-	-	-	5	-	Ω		
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)	-	0	0	18	±100 (Note 2)		±1000 (Note 2)		-	±0.01	±100 (Note 2)	nA		
Capacitance:	-	-5	5-	5										
Input, C _{IS}					-	-	-	-	-	-	-	5	-	pF
Output, C _{OS}														
CD4051					-	-	-	-	-	-	-	30	-	pF
CD4052					-	-	-	-	-	-	-	18	-	pF
CD4053	-	-	-	-	-	-	-	9	-	pF				
Feedthrough C _{IOS}														
C _{IOS}														
Propagation Delay Time (Signal Input to Output)		V _{DD}	R _L = 200kΩ, C _L = 50pF, t _r , t _f = 20ns	5	-	-	-	-	-	30	60	ns		
				10	-	-	-	-	-	15	30	ns		
				15	-	-	-	-	-	10	20	ns		

CD4051B, CD4052B, CD4053B

Electrical Specifications Common Conditions Here: If Whole Table is For the Full Temp. Range, $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)** (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	-55	-40	85	125	25			
									MIN	TYP	MAX	
CONTROL (ADDRESS OR INHIBIT), V_C												
Input Low Voltage, V_{IL} , Max	$V_{IL} = V_{DD}$ through 1k Ω ; $V_{IH} = V_{DD}$ through 1k Ω	$V_{EE} = V_{SS}$, $R_L = 1k\Omega$ to V_{SS} , $I_{IS} < 2\mu A$ on All OFF Channels	5	1.5	1.5	1.5	1.5	-	-	1.5	V	
			10	3	3	3	3	-	-	3	V	
			15	4	4	4	4	-	-	4	V	
Input High Voltage, V_{IH} , Min	$V_{IL} = V_{DD}$ through 1k Ω ; $V_{IH} = V_{DD}$ through 1k Ω	$V_{EE} = V_{SS}$, $R_L = 1k\Omega$ to V_{SS} , $I_{IS} < 2\mu A$ on All OFF Channels	5	3.5	3.5	3.5	3.5	3.5	-	-	V	
			10	7	7	7	7	7	-	-	V	
			15	11	11	11	11	11	-	-	V	
Input Current, I_{IN} (Max)	$V_{IN} = 0, 18$		18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1	μA	
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figures 10, 11, 14	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	450	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-5	0	5	-	-	-	-	-	225	450	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning ON) See Figure 11	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 1k\Omega$	0	0	5	-	-	-	-	-	400	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-10	0	5	-	-	-	-	-	200	400	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning OFF) See Figure 15	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	200	450	ns
		0	0	10	-	-	-	-	-	90	210	ns
		0	0	15	-	-	-	-	-	70	160	ns
		-10	0	5	-	-	-	-	-	130	300	ns
Input Capacitance, C_{IN} (Any Address or Inhibit Input)				-	-	-	-	-	5	7.5	pF	

NOTE:

- Determined by minimum feasible leakage measurement for automatic testing.

Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS		UNITS	
	V_{IS} (V)	V_{DD} (V)	R_L (k Ω)	TYP			
Cutoff (-3dB) Frequency Channel ON (Sine Wave Input)	5 (Note 3)	10	1	V_{OS} at Common OUT/IN	CD4053	30	MHz
					CD4052	25	MHz
					CD4051	20	MHz
				$V_{EE} = V_{SS}$, $20\text{Log} \frac{V_{OS}}{V_{IS}} = -3\text{dB}$	V_{OS} at Any Channel	60	MHz

Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS			
	V _{IS} (V)	V _{DD} (V)	R _L (kΩ)	TYP	UNITS		
Total Harmonic Distortion, THD	2 (Note 3)	5	10	0.3	%		
	3 (Note 3)	10		0.2	%		
	5 (Note 3)	15		0.12	%		
	V _{EE} = V _{SS} , f _{IS} = 1kHz Sine Wave				%		
-40dB Feedthrough Frequency (All Channels OFF)	5 (Note 3)	10	1	V _{OS} at Common OUT/IN	CD4053	8	MHz
	V _{EE} = V _{SS} , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$				CD4052	10	MHz
					CD4051	12	MHz
				V _{OS} at Any Channel	8	MHz	
-40dB Signal Crosstalk Frequency	5 (Note 3)	10	1	Between Any 2 Channels		3	MHz
	V _{EE} = V _{SS} , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$			Between Sections, CD4052 Only	Measured on Common	6	MHz
					Measured on Any Channel	10	MHz
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	MHz
					In Pin 15, Out Pin 14	6	MHz
Address-or-Inhibit-to-Signal Crosstalk	-	10	10 (Note 4)			65	mV _{PEAK}
	V _{EE} = 0, V _{SS} = 0, t _r , t _f = 20ns, V _{CC} = V _{DD} - V _{SS} (Square Wave)					65	mV _{PEAK}

NOTES:

3. Peak-to-Peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$
4. Both ends of channel.

Typical Performance Curves

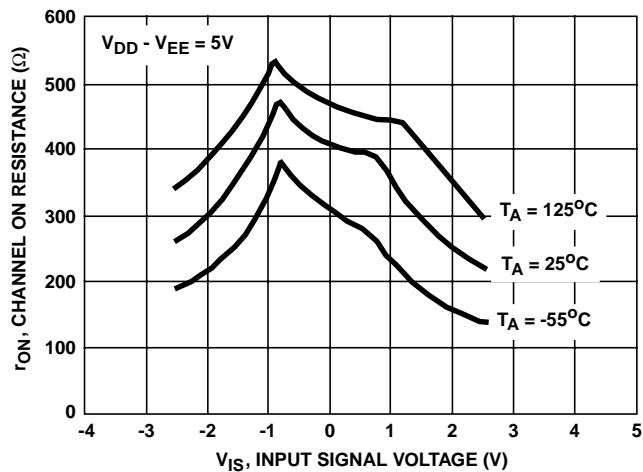


FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)



FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Curves (Continued)

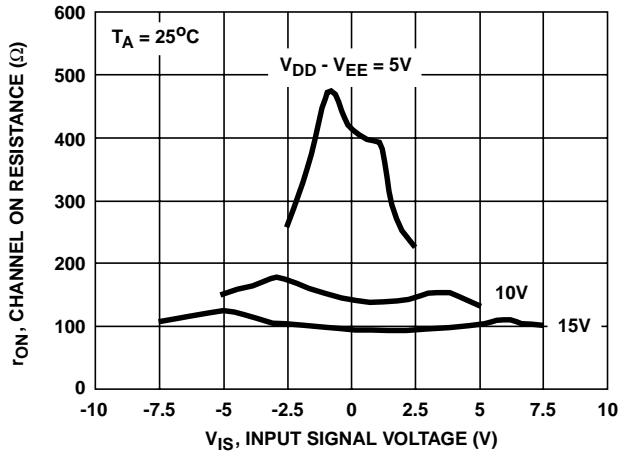


FIGURE 3. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

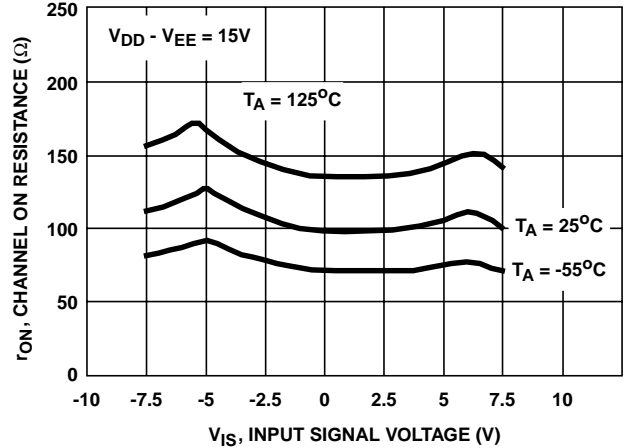


FIGURE 4. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

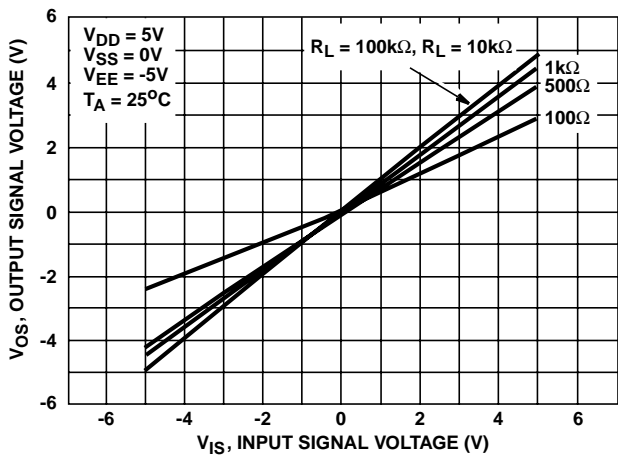


FIGURE 5. ON CHARACTERISTICS FOR 1 OF 8 CHANNELS (CD4051B)

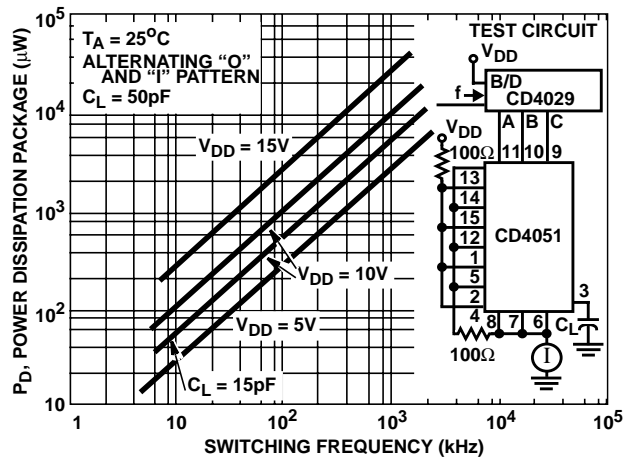


FIGURE 6. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4051B)

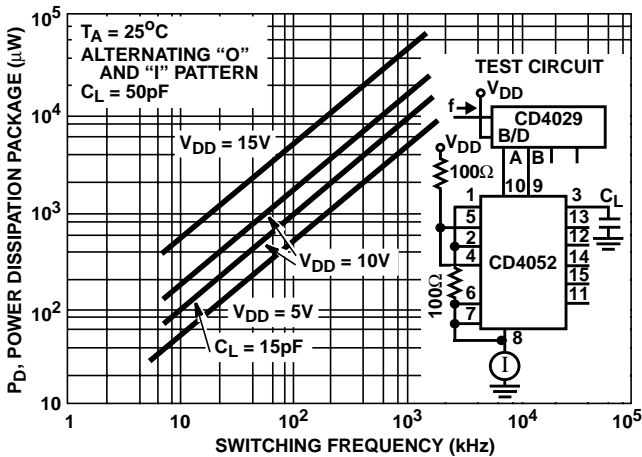


FIGURE 7. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4052B)

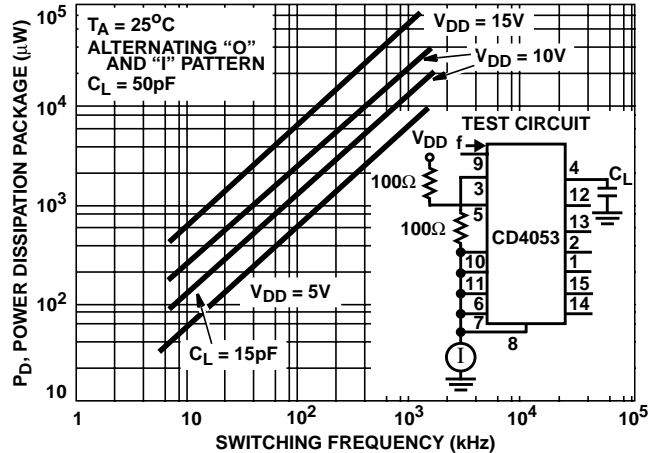


FIGURE 8. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4053B)

Test Circuits and Waveforms



NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD} . The analog signal (through the TG) may swing from V_{EE} to V_{DD} .

FIGURE 9. TYPICAL BIAS VOLTAGES



FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON ($R_L = 1k\Omega$)



FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF ($R_L = 1k\Omega$)



FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF

Test Circuits and Waveforms (Continued)

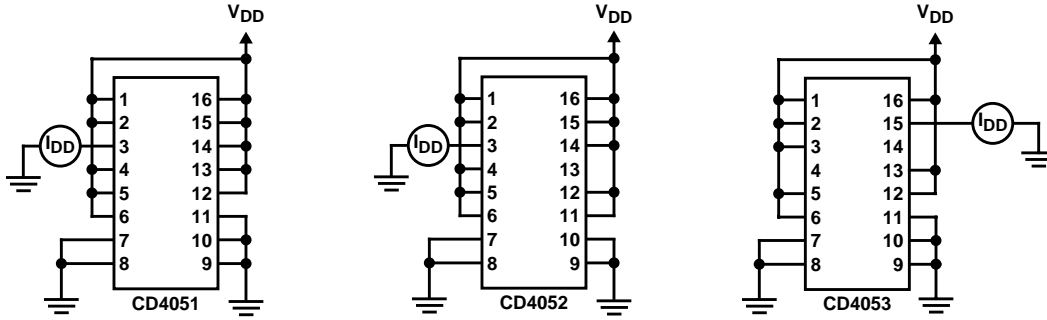


FIGURE 13. OFF CHANNEL LEAKAGE CURRENT - ALL CHANNELS OFF

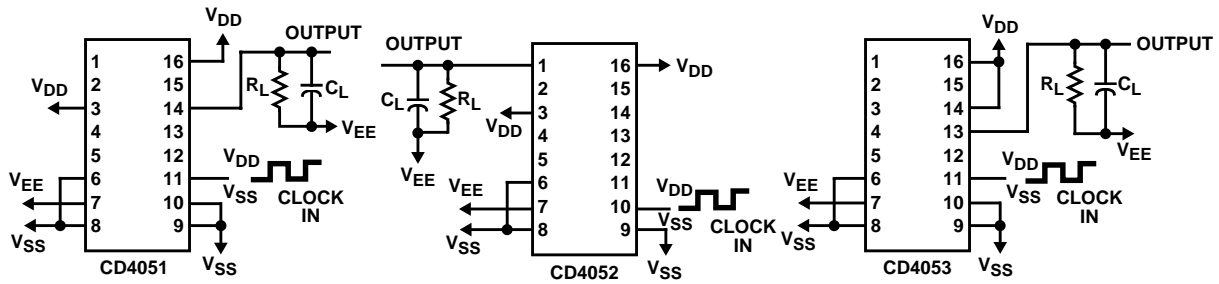


FIGURE 14. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT

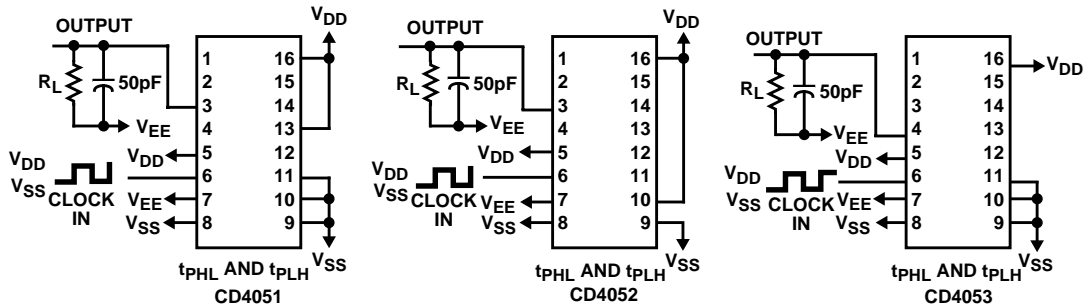
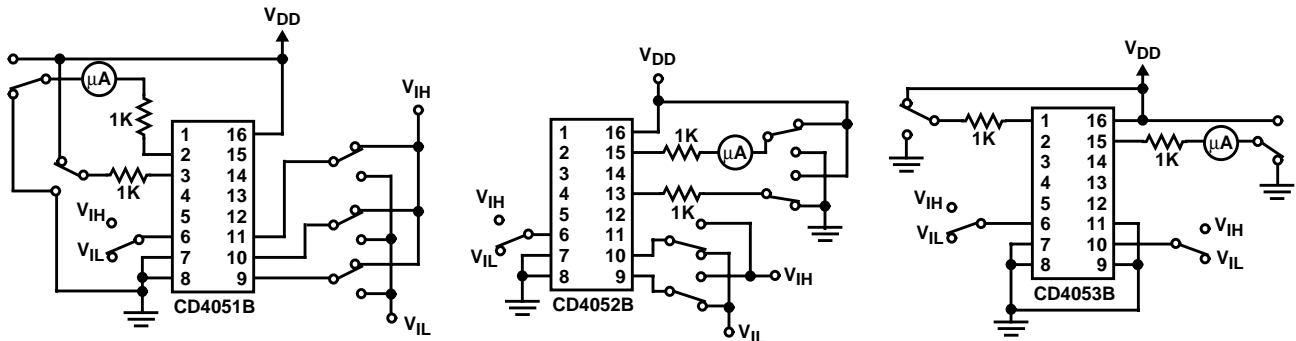


FIGURE 15. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT



MEASURE $< 2\mu\text{A}$ ON ALL "OFF" CHANNELS (e.g., CHANNEL 6)

MEASURE $< 2\mu\text{A}$ ON ALL "OFF" CHANNELS (e.g., CHANNEL 2x)

MEASURE $< 2\mu\text{A}$ ON ALL "OFF" CHANNELS (e.g., CHANNEL by)

FIGURE 16. INPUT VOLTAGE TEST CIRCUITS (NOISE IMMUNITY)

Test Circuits and Waveforms (Continued)

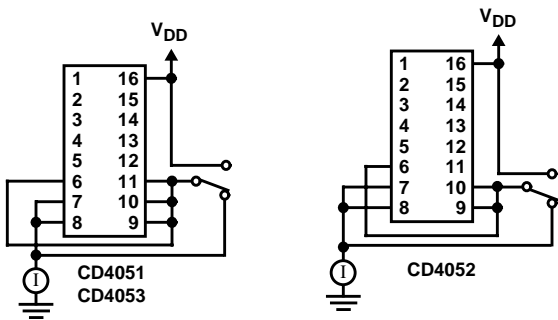


FIGURE 17. QUIESCENT DEVICE CURRENT



FIGURE 18. CHANNEL ON RESISTANCE MEASUREMENT CIRCUIT

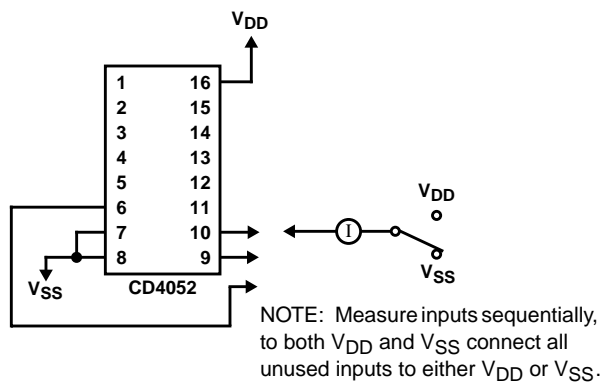
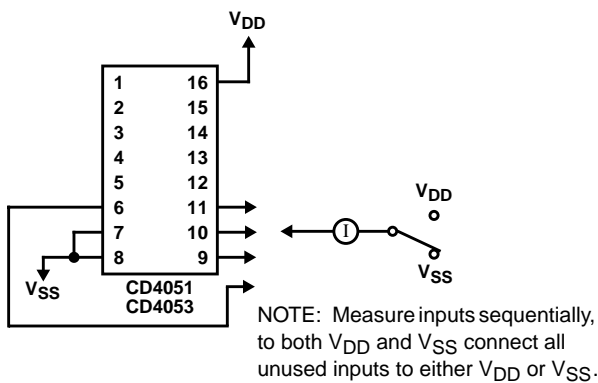


FIGURE 19. INPUT CURRENT



FIGURE 20. FEEDTHROUGH (ALL TYPES)

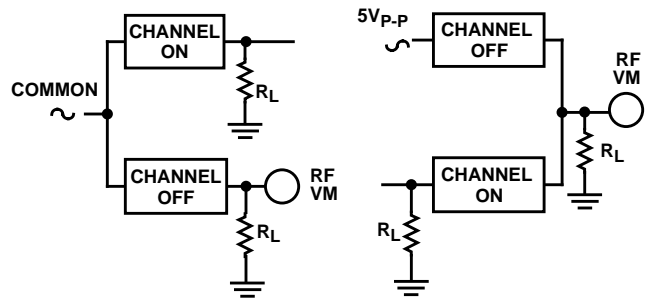


FIGURE 21. CROSSTALK BETWEEN ANY TWO CHANNELS (ALL TYPES)

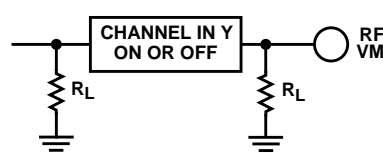
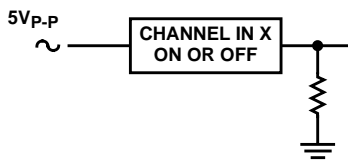


FIGURE 22. CROSSTALK BETWEEN DUALS OR TRIPLETS (CD4052B, CD4053B)

Test Circuits and Waveforms (Continued)



FIGURE 23. TYPICAL TIME-DIVISION APPLICATION OF THE CD4052B

Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L ($R_L =$ effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.



FIGURE 24. 24-TO-1 MUX ADDRESSING

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
7901502EA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
8101801EA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4051BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4051BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4051BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4051BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
CD4051BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
CD4051BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
CD4051BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4051BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4051BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4052BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4052BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4052BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4052BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4052BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4052BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4052BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4052BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4052BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4053BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4053BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4053BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4053BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4053BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4053BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4053BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4053BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4053BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

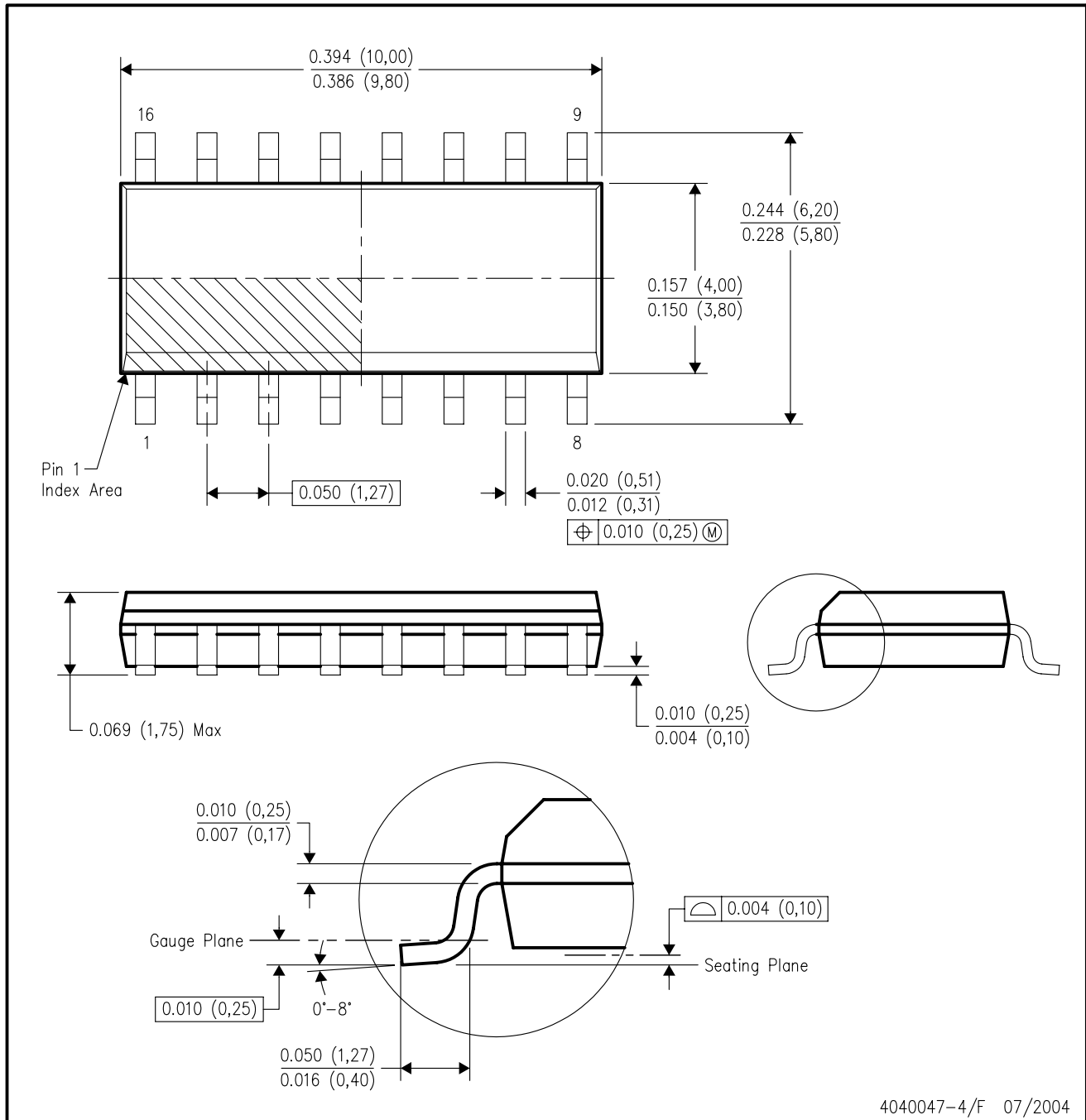
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265