

CD4069UB CMOS Hex Inverter

1 Features

- Standardized Symmetrical Output Characteristics
- Medium Speed Operation: $-t_{PHL}$, $t_{PLH} = 30$ ns at 10 V (Typical)
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 μ A at 18 V Over Full Package-Temperature Range, 100 nA at 18 V and 25°C
- Meets All Requirements of JEDEC Tentative Standard No. 13B, *Standard Specifications for Description of B Series CMOS Devices*

2 Applications

- Logic Inversion
- Pulse Shaping
- Oscillators
- High-Input-Impedance Amplifiers

3 Description

The CD4069UB device consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 hex inverter and buffers are not required.

Device Information⁽¹⁾

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
CD4069UBE	PDIP (14)	19.30 mm × 6.35 mm
CD4069UBF	CDIP (14)	19.56 mm × 6.67 mm
CD4069UBM	SOIC (14)	8.65 mm × 3.91 mm
CD4069UBNSR	SO (14)	10.30 mm × 5.30 mm
CD4069UBPW	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

CD4069UB Functional Diagram

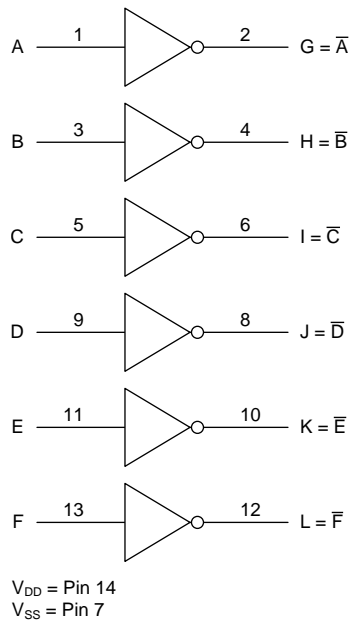


Table of Contents

1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Pin Configuration and Functions 3 6 Specifications 4 6.1 Absolute Maximum Ratings 4 6.2 ESD Ratings 4 6.3 Recommended Operating Conditions..... 4 6.4 Thermal Information 4 6.5 Electrical Characteristics – Dynamic..... 5 6.6 Electrical Characteristics – Static..... 5 6.7 Typical Characteristics 8 7 Parameter Measurement Information 9 8 Detailed Description 13 8.1 Overview 13 8.2 Functional Block Diagram 13	8.3 Feature Description 13 8.4 Device Functional Modes 13 9 Application and Implementation 14 9.1 Application Information 14 9.2 Typical Application 14 10 Power Supply Recommendations 16 11 Layout 16 11.1 Layout Guidelines 16 11.2 Layout Example 16 12 Device and Documentation Support 17 12.1 Device Support..... 17 12.2 Documentation Support 17 12.3 Community Resource..... 17 12.4 Trademarks 17 12.5 Electrostatic Discharge Caution..... 17 12.6 Glossary 17 13 Mechanical, Packaging, and Orderable Information 17
---	--

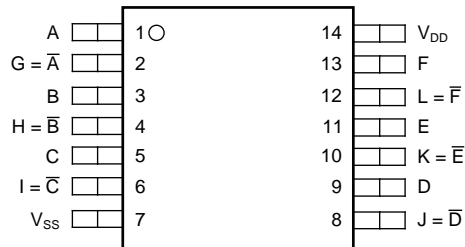
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2003) to Revision D	Page
<ul style="list-style-type: none"> • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

5 Pin Configuration and Functions

D, J, N, NS, and PW Packages
14-Pin PDIP, CDIP, SOIC, SO, and TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	A input
B	3	I	B input
C	5	I	C input
D	9	I	D input
E	11	I	E input
F	13	I	F input
$G = \bar{A}$	2	O	G output
$H = \bar{B}$	4	O	H output
$I = \bar{C}$	6	O	I output
$J = \bar{D}$	8	O	J output
$K = \bar{E}$	10	O	K output
$L = \bar{F}$	12	O	L output
V_{DD}	14	—	Positive supply
V_{SS}	7	—	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	DC supply-voltage (voltages referenced to V _{SS} terminal)	-0.5	20	V
V _I	Input voltage, all inputs	-0.5 to V _{DD}	0.5	V
I _{IK}	DC input current, any one input	-10	10	mA
P _D	Power dissipation per package	-55°C to 100°C	500	mW
		100°C to 125°C	12	
	Device dissipation per output transistor	Full range (all package types)		100
Lead temperature ⁽²⁾			265	°C
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) During soldering at distance 1/16 inch ± 1/32 inch (1.59 mm ± 0.79 mm) from case for 10 s maximum

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{DD}	Supply voltage	3	18	V
T _A	Operating temperature	-55	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	CD4069UB					UNIT	
	D (SOIC)	J (CDIP)	N (PDIP)	NS (SO)	PW (TSSOP)		
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	94.9	—	57.9	91.2	122.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.4	28.5	45.5	48.8	50.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	49.2	—	37.7	50	63.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	21.1	—	30.6	15	6.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	48.9	—	37.6	49.6	63.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics – Dynamic

 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay time	$V_{DD} (V) = 5$		55	110	ns
	$V_{DD} (V) = 10$		30	60	
	$V_{DD} (V) = 15$		25	50	
t_{THL}, t_{TLH} Transition time	$V_{DD} (V) = 5$		100	200	ns
	$V_{DD} (V) = 10$		50	100	
	$V_{DD} (V) = 15$		40	80	
C_{IN} Input capacitance	Any input		10	15	pF

6.6 Electrical Characteristics – Static

 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I_{DDmax} Quiescent device current	$V_{IN} = 0\text{V or } 5\text{ V}, V_{DD} = 5\text{ V}$	$T_A = -55^\circ\text{C}$		0.25	μA	
		$T_A = -40^\circ\text{C}$		0.25		
		$T_A = 25^\circ\text{C}$	0.01	0.25		
		$T_A = 85^\circ\text{C}$		7.5		
		$T_A = 125^\circ\text{C}$		7.5		
	$V_{IN} = 0\text{ or } 10\text{ V}, V_{DD} = 10\text{ V}$	$T_A = -55^\circ\text{C}$				0.5
		$T_A = -40^\circ\text{C}$				0.5
		$T_A = 25^\circ\text{C}$	0.01	0.5		
		$T_A = 85^\circ\text{C}$		15		
		$T_A = 125^\circ\text{C}$		15		
	$V_{IN} = 0\text{ or } 15\text{ V}, V_{DD} = 15\text{ V}$	$T_A = -55^\circ\text{C}$				1
		$T_A = -40^\circ\text{C}$				1
		$T_A = 25^\circ\text{C}$	0.01	1		
		$T_A = 85^\circ\text{C}$		30		
		$T_A = 125^\circ\text{C}$		30		
$V_{IN} = 0\text{ or } 20\text{ V}, V_{DD} = 20\text{ V}$	$T_A = -55^\circ\text{C}$			5		
	$T_A = -40^\circ\text{C}$			5		
	$T_A = 25^\circ\text{C}$	0.02	5			
	$T_A = 85^\circ\text{C}$		150			
	$T_A = 125^\circ\text{C}$		150			
I_{OLmin} Output low (sink) current	$V_O = 0.4\text{ V}, V_{IN} = 5\text{ V}, V_{DD} = 5\text{ V}$	$T_A = -55^\circ\text{C}$	0.64		mA	
		$T_A = -40^\circ\text{C}$	0.61			
		$T_A = 25^\circ\text{C}$	0.51	1		
		$T_A = 85^\circ\text{C}$	0.42			
		$T_A = 125^\circ\text{C}$	0.36			
	$V_O = 0.5\text{ V}, V_{IN} = 10\text{ V}, V_{DD} = 10\text{ V}$	$T_A = -55^\circ\text{C}$	1.6			
		$T_A = -40^\circ\text{C}$	1.5			
		$T_A = 25^\circ\text{C}$	1.3	2.6		
		$T_A = 85^\circ\text{C}$	1.1			
		$T_A = 125^\circ\text{C}$	0.9			
	$V_O = 1.5\text{ V}, V_{IN} = 15\text{ V}, V_{DD} = 15\text{ V}$	$T_A = -55^\circ\text{C}$	4.2			
		$T_A = -40^\circ\text{C}$	4			
		$T_A = 25^\circ\text{C}$	3.4	6.8		
		$T_A = 85^\circ\text{C}$	2.8			
		$T_A = 125^\circ\text{C}$	2.4			

Electrical Characteristics – Static (continued)
 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20$ ns; $C_L = 50$ pF; $R_L = 200$ k Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I_{OHmin}	Output high (source) current	$V_O = 4.6$ V, $V_{IN} = 0$ V, $V_{DD} = 5$ V	$T_A = -55^\circ\text{C}$	-0.64			mA
			$T_A = -40^\circ\text{C}$	-0.61			
			$T_A = 25^\circ\text{C}$	-0.51	-1		
			$T_A = 85^\circ\text{C}$	-0.42			
			$T_A = 125^\circ\text{C}$	-0.36			
		$V_O = 2.5$ V, $V_{IN} = 0$ V, $V_{DD} = 5$ V	$T_A = -55^\circ\text{C}$	-2			
			$T_A = -40^\circ\text{C}$	-1.8			
			$T_A = 25^\circ\text{C}$	-1.6	-3.2		
			$T_A = 85^\circ\text{C}$	-1.3			
			$T_A = 125^\circ\text{C}$	-1.15			
		$V_O = 9.5$ V, $V_{IN} = 0$ V, $V_{DD} = 10$ V	$T_A = -55^\circ\text{C}$	-1.6			
			$T_A = -40^\circ\text{C}$	-1.5			
			$T_A = 25^\circ\text{C}$	-1.3	-2.6		
			$T_A = 85^\circ\text{C}$	-1.1			
			$T_A = 125^\circ\text{C}$	-0.9			
		$V_O = 13.5$ V, $V_{IN} = 0$ V, $V_{DD} = 15$ V	$T_A = -55^\circ\text{C}$	-4.2			
$T_A = -40^\circ\text{C}$	-4						
$T_A = 25^\circ\text{C}$	-3.4		-6.8				
$T_A = 85^\circ\text{C}$	-2.8						
$T_A = 125^\circ\text{C}$	-2.4						
V_{OLmax}	Low-level output voltage	$V_{IN} = 5$ V, $V_{DD} = 5$ V	$T_A = 25^\circ\text{C}$		0	0.05	V
			All other temperatures			0.05	
		$V_{IN} = 10$ V, $V_{DD} = 10$ V	$T_A = 25^\circ\text{C}$		0	0.05	
			All other temperatures			0.05	
		$V_{IN} = 15$ V, $V_{DD} = 15$ V	$T_A = 25^\circ\text{C}$		0	0.05	
			All other temperatures			0.05	
V_{OHmin}	High-level output voltage	$V_{IN} = 0$ V, $V_{DD} = 5$ V	$T_A = 25^\circ\text{C}$	4.95	5		V
			All other temperatures	4.95			
		$V_{IN} = 0$ V, $V_{DD} = 10$ V	$T_A = 25^\circ\text{C}$	9.95	10		
			All other temperatures	9.95			
		$V_{IN} = 0$ V, $V_{DD} = 15$ V	$T_A = 25^\circ\text{C}$	14.95	15		
			All other temperatures	14.95			
V_{ILmax}	Input low voltage	$V_O = 4.5$ V, $V_{DD} = 5$ V, all temperatures				1	V
		$V_O = 9$ V, $V_{DD} = 10$ V, all temperatures				2	
		$V_O = 13.5$ V, $V_{DD} = 15$ V, all temperatures				2.5	
V_{IHmin}	Input high voltage	$V_O = 0.5$ V, $V_{DD} = 5$ V, all temperatures			4		V
		$V_O = 1$ V, $V_{DD} = 10$ V, all temperatures			8		
		$V_O = 1.5$ V, $V_{DD} = 15$ V, all temperatures			12.5		

Electrical Characteristics – Static (continued)
 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{INmax} Input current	$V_{IN} = 0\text{ V to }18\text{ V}, V_{DD} = 18\text{ V}$	$T_A = -55^\circ\text{C}$		± 01	μA
		$T_A = -40^\circ\text{C}$		± 01	
		$T_A = 25^\circ\text{C}$		$\pm 10^{-5}$	
		$T_A = 85^\circ\text{C}$		± 1	
		$T_A = 125^\circ\text{C}$		± 1	

6.7 Typical Characteristics

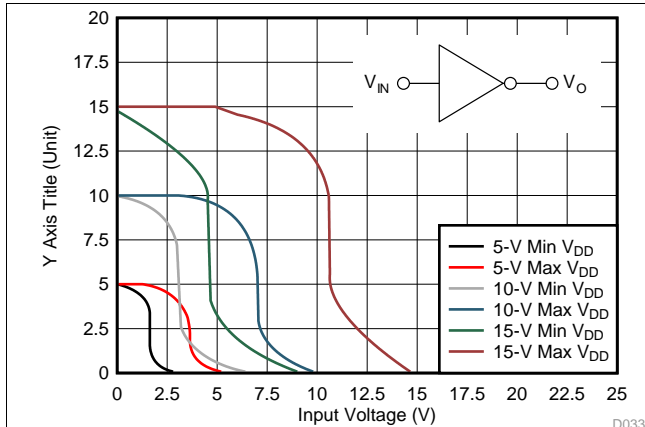


Figure 1. Minimum and Maximum Voltage Transfer Characteristics

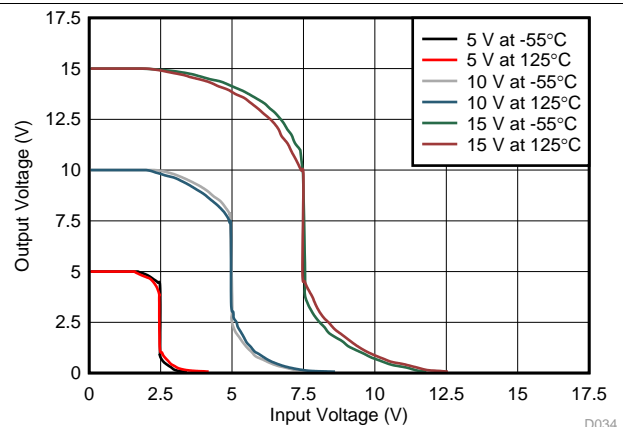


Figure 2. Typical Voltage Transfer Characteristics as a Function of Temperature

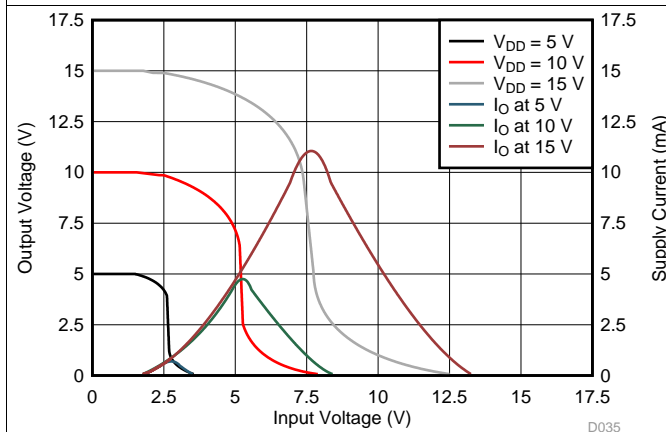


Figure 3. Typical Current and Voltage Transfer Characteristics

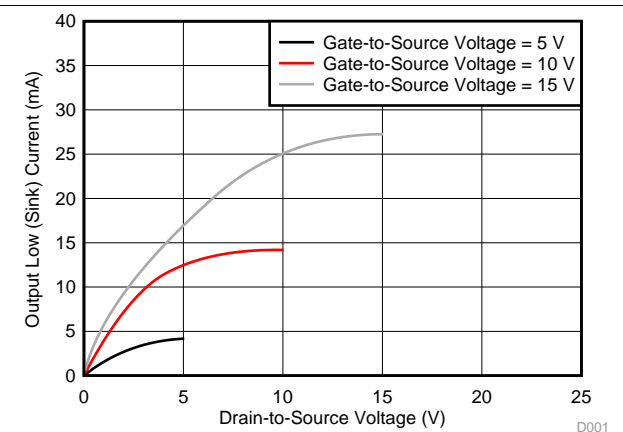


Figure 4. Typical Output Low (Sink) Current Characteristics

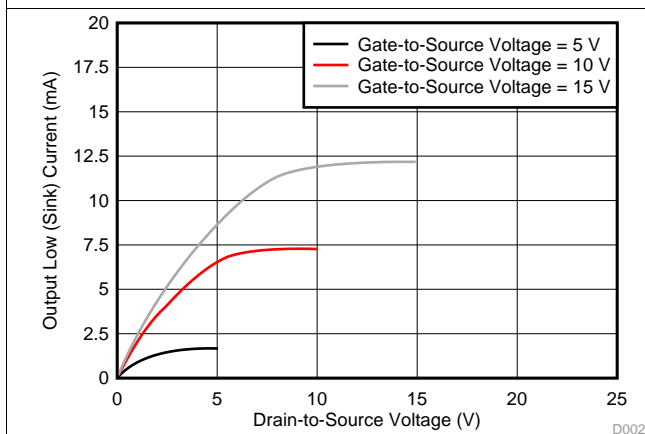


Figure 5. Minimum Output Low (Sink) Current Characteristics

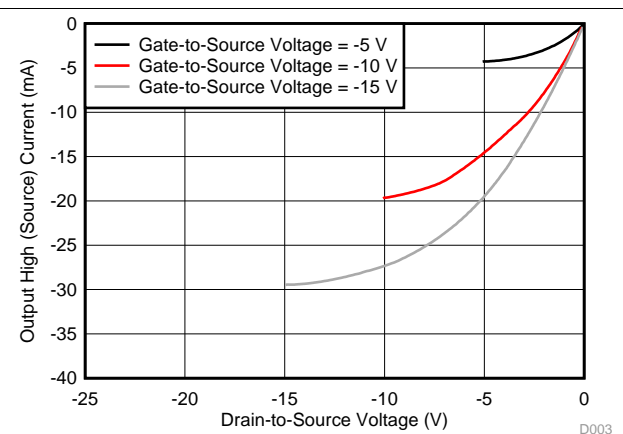
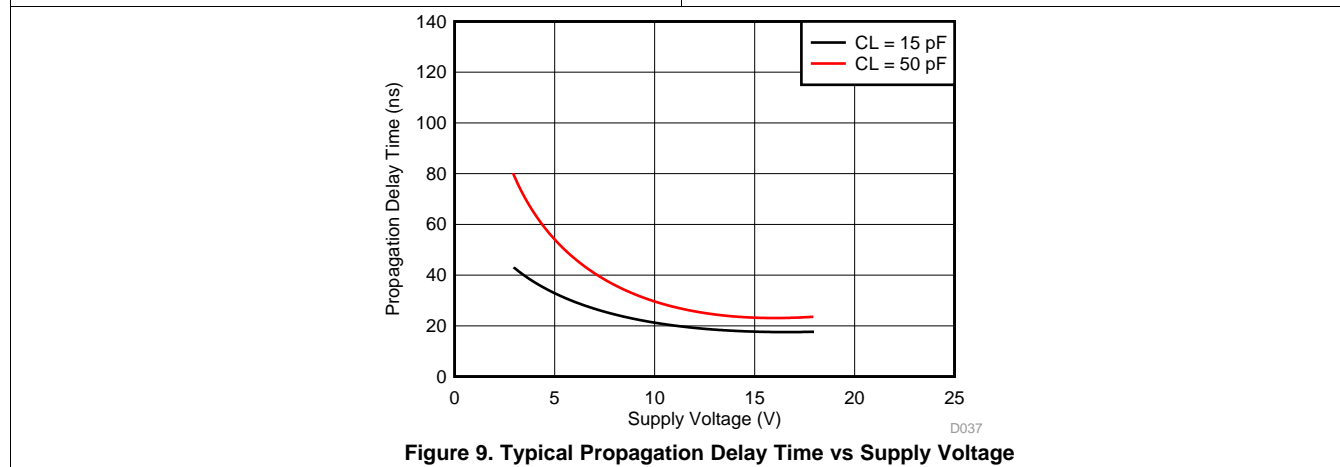
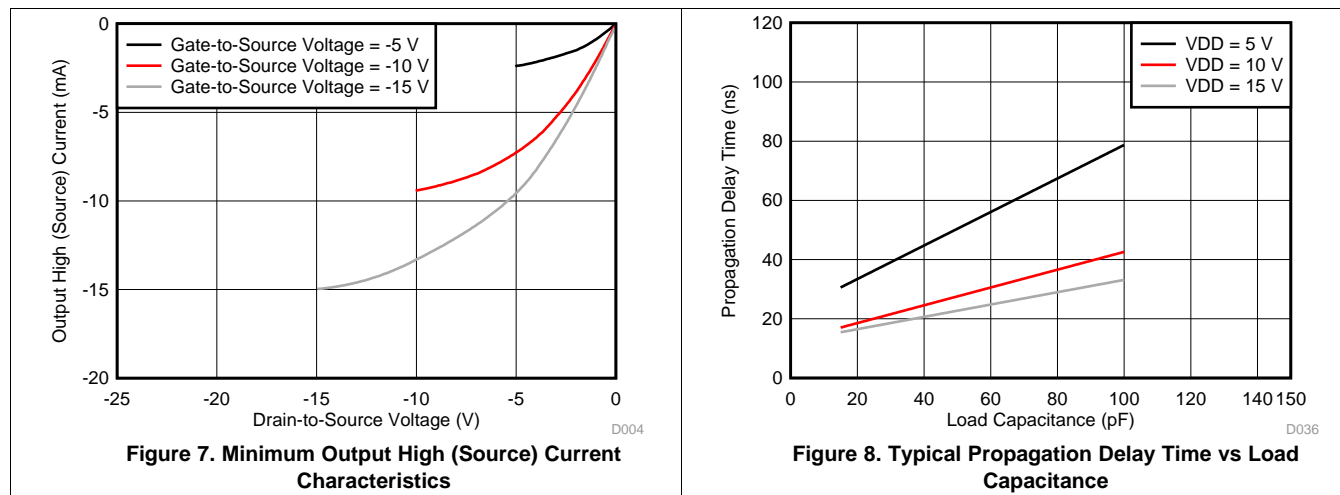


Figure 6. Typical Output High (Source) Current Characteristics

Typical Characteristics (continued)



7 Parameter Measurement Information

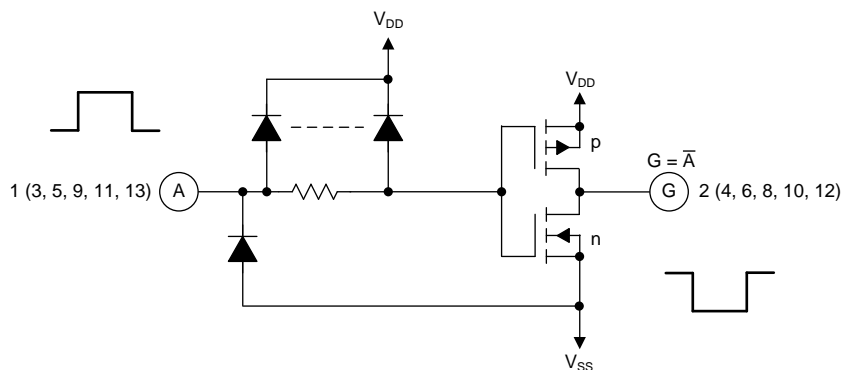


Figure 10. Schematic Diagram of One of Six Identical Inverters

Parameter Measurement Information (continued)

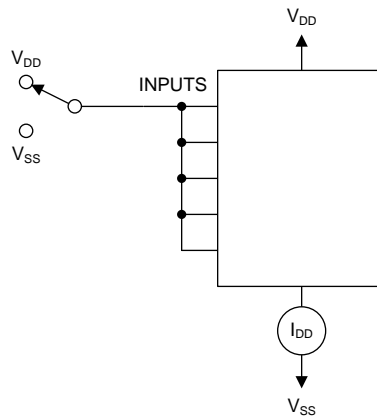


Figure 11. Quiescent Device Current Test Circuit

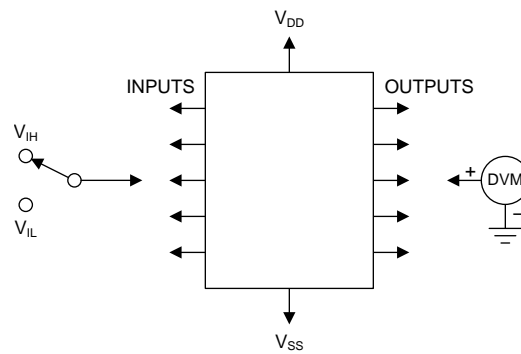


Figure 12. Noise Immunity Test Circuit

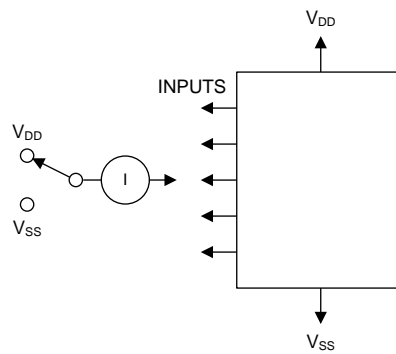


Figure 13. Input Leakage Current Test Circuit

Parameter Measurement Information (continued)

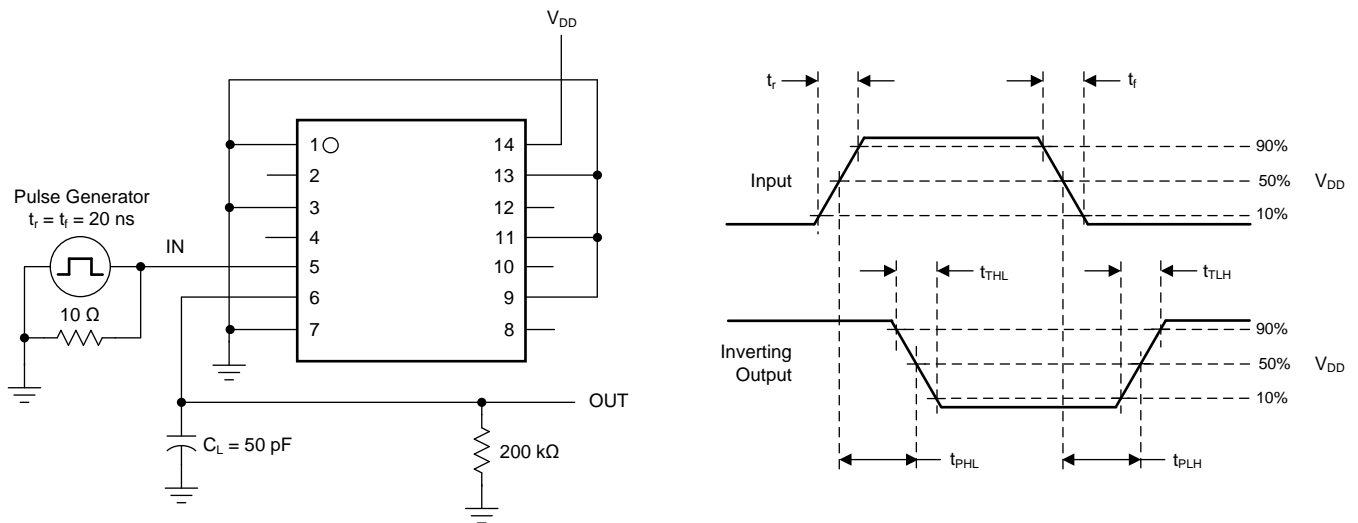


Figure 14. Dynamic Electrical Characteristics Test Circuit and Waveform

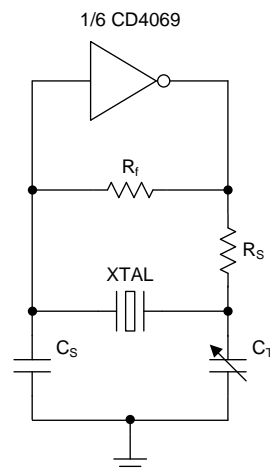


Figure 15. Typical Crystal Oscillator Circuit

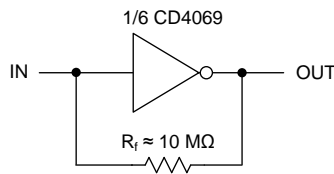


Figure 16. High-Input Impedance Amplifier

Parameter Measurement Information (continued)

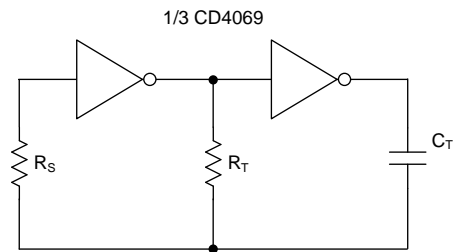
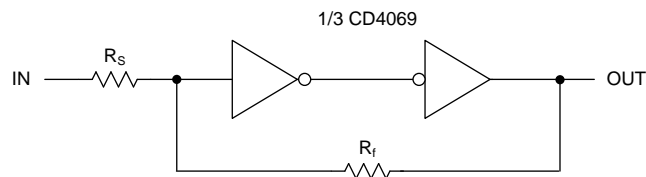


Figure 17. Typical RC Oscillator Circuit



Upper Switching Point :

$$V_P = \frac{R_S + R_f}{R_f} \times \frac{V_{DD}}{2}$$

Lower Switching Point :

$$V_N = \frac{R_f - R_S}{R_f} \times \frac{V_{DD}}{2}$$

$$R_f > R_S$$

Figure 18. Input Pulse Shaping Circuit

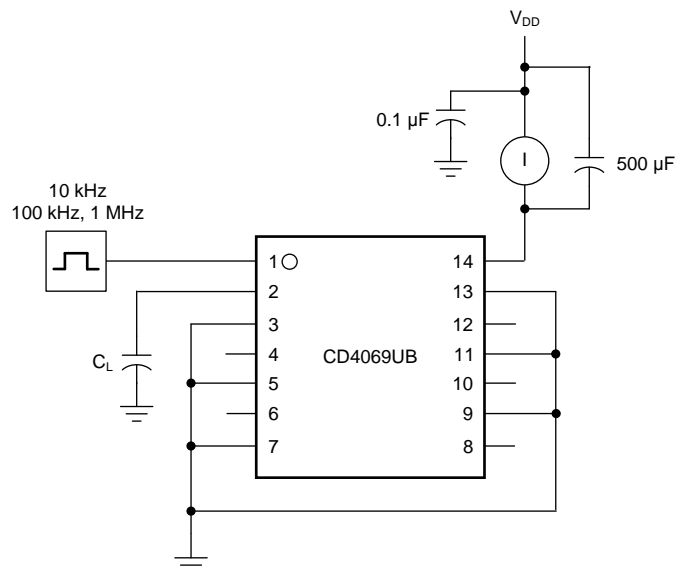


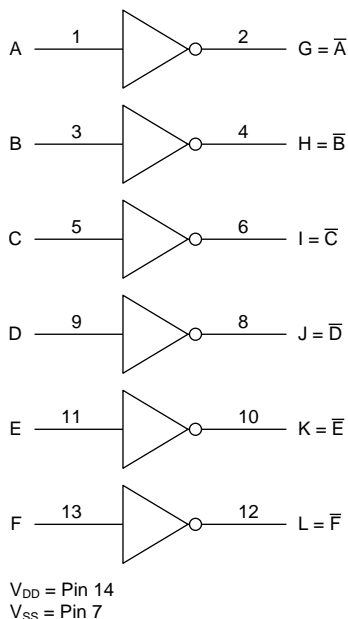
Figure 19. Dynamic Power Dissipation Test Circuit

8 Detailed Description

8.1 Overview

The CD4069UB device has six inverter circuits. The recommended operating range is from 3 V to 18 V. The CD4069UB-series types are supplied in 14-pin hermetic dual-in-line ceramic packages (F3A suffix), 14-pin dual-in-line plastic packages (E suffix), 14-pin small-outline packages (M, MT, M96, and NSR suffixes), and 14-pin thin shrink small-outline packages (PW and PWR suffixes).

8.2 Functional Block Diagram



8.3 Feature Description

CD4069UB has standardized symmetrical output characteristics and a wide operating voltage range from 3 V to 18 V with quiescent current tested at 20 V. This has a medium operation speed $-t_{PHL}, t_{PLH} = 30$ ns (typical) at 10 V. The operating temperature is from -55°C to 125°C . CD4069UB meets all requirements of JEDEC tentative standard No. 13B, *Standard Specifications for Description of B Series CMOS Devices*.

8.4 Device Functional Modes

Table 1 shows the functional modes for CD4069UB.

Table 1. Function Table

INPUT A, B, C, D, E, F	OUTPUT G, H, I, J, K, L
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CD4069UB device has a low input current of 1 μA at 18 V over full package-temperature range and 100 nA at 18 V, 25°C. This device has a wide operating voltage range from 3 V to 18 V and used in high voltage applications.

9.2 Typical Application

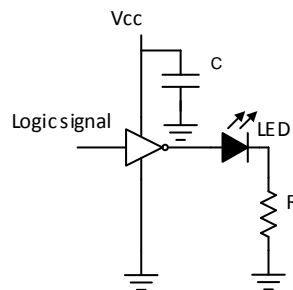


Figure 20. CD4069UB Application

9.2.1 Design Requirements

The CD4069UB device is the industry's highest logic inverter operating at 18 V under recommended conditions. The lower drive capabilities makes it suitable for driving light loads like LED and greatly reduces chances of overshoots and undershoots.

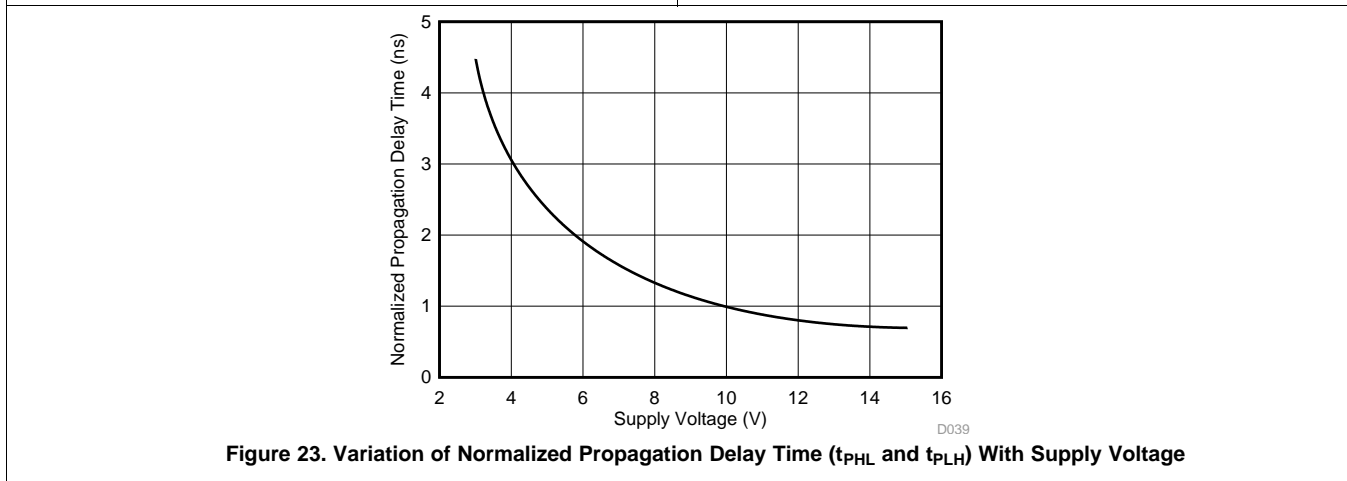
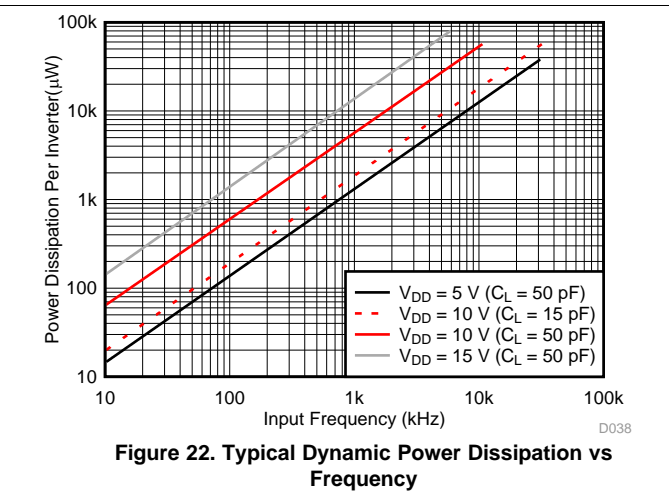
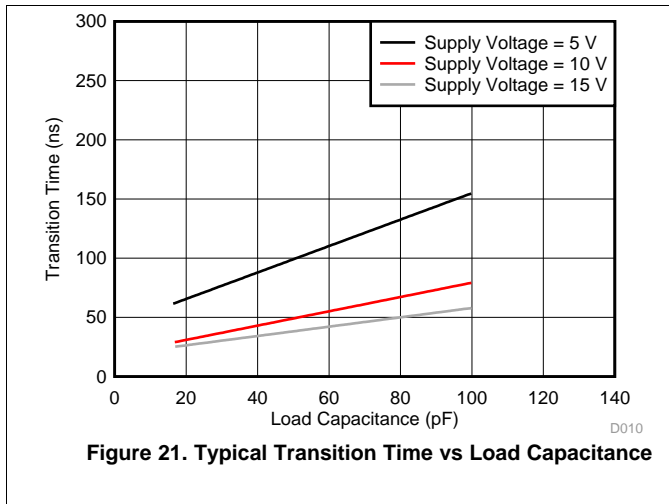
9.2.2 Detailed Design Procedure

The recommended input conditions for [Figure 20](#) includes rise time and fall time specifications (see $\Delta t/\Delta V$ in [Recommended Operating Conditions](#)) and specified high and low levels (see V_{IH} and V_{IL} in [Recommended Operating Conditions](#)). Inputs are not overvoltage tolerant and must be below V_{CC} level because of the presence of input clamp diodes to V_{CC} .

The recommended output condition for the CD4069UB application includes specific load currents. Load currents must be limited so as to not exceed the total power (continuous current through V_{CC} or GND) for the device. These limits are located in the [Absolute Maximum Ratings](#). Outputs must not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μF capacitor. If there are multiple V_{CC} pins, then TI recommends a 0.01- μF or 0.022- μF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

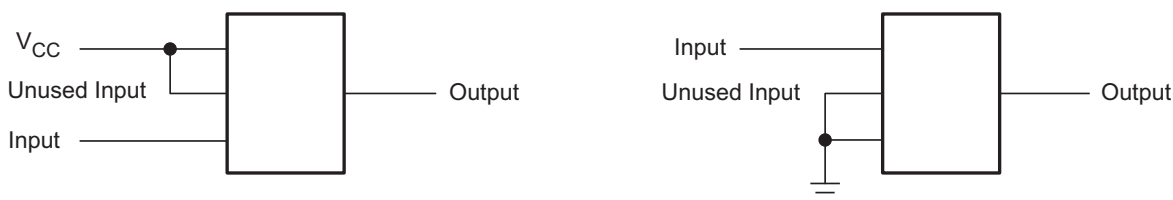
11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, digital logic device functions or parts of these functions are unused (for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. This rule must be observed under all circumstances specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. See the application note, [Implications of Slow or Floating CMOS Inputs \(SCBA004\)](#), for more information on the effects of floating inputs. The logic level must apply to any particular unused input depending on the function of the device. Generally, they are tied to GND or V_{CC} (whichever is convenient).

11.2 Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4069UBE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4069UBE	Samples
CD4069UBEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4069UBE	Samples
CD4069UBF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4069UBF	Samples
CD4069UBF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4069UBF3A	Samples
CD4069UBM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBM96G4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		
CD4069UBMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM	Samples
CD4069UBNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UB	Samples
CD4069UBNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UB	Samples
CD4069UBPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
CD4069UBPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB	Samples
JM38510/17401BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 17401BCA	Samples
M38510/17401BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 17401BCA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4069UB, CD4069UB-MIL :

● Catalog: [CD4069UB](#)

● Military: [CD4069UB-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4069UBM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4069UBM96	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
CD4069UBMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4069UBNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4069UBPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4069UBPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4069UBM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4069UBM96	SOIC	D	14	2500	364.0	364.0	27.0
CD4069UBMT	SOIC	D	14	250	367.0	367.0	38.0
CD4069UBNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4069UBPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD4069UBPWR	TSSOP	PW	14	2000	364.0	364.0	27.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com