

CMOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

■ CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

Features:

- 3-state parallel outputs for connection to common bus
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Medium speed operation – 5 MHz at 10 V (typ.)
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range):
1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V
2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications

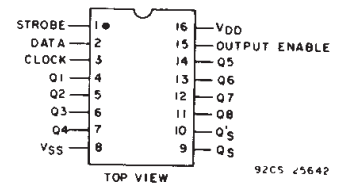
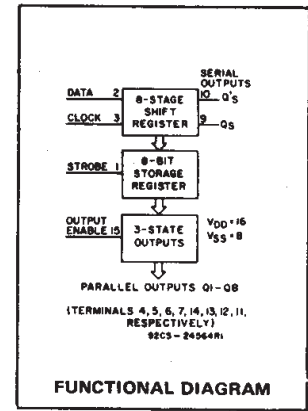


Fig. 1 – Terminal assignment.

MAXIMUM RATINGS, Absolute-Maximum Values:

| | | |
|---|-------|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | | -0.5V to +20V |
| Voltages referenced to V _{SS} Terminal) | | |
| INPUT VOLTAGE RANGE, ALL INPUTS | | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | | |
| For T _A = -55°C to +100°C | | 500mW |
| For T _A = +100°C to +125°C | | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | | +265°C |

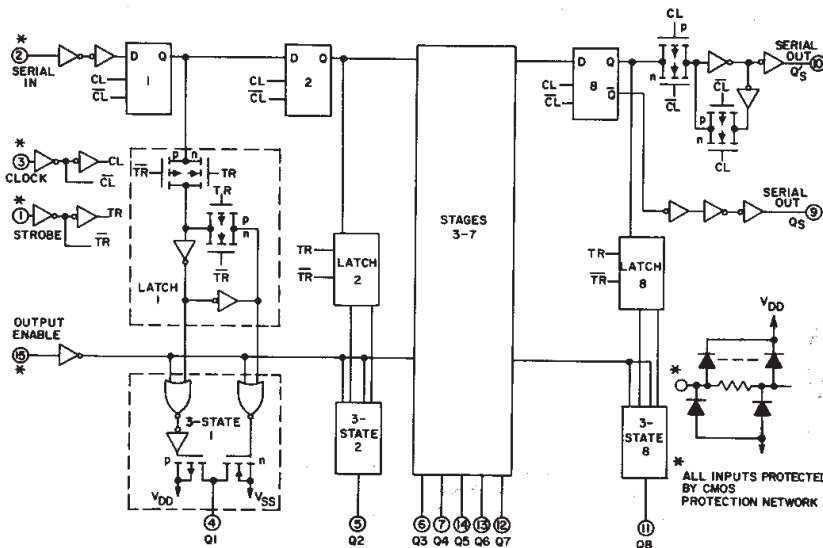


Fig. 2 – CD4094B Logic diagram.

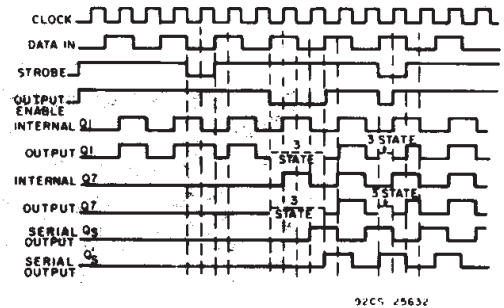


Fig. 3 – Timing diagram.

CD4094B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | VDD (V) | LIMITS | | UNITS |
|--|---------------|------------------|------------------|---------------|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For T_A =Full Package-Temperature Range) | | 3 | 18 | V |
| Data Setup Time, t_S | 5 10 15 | 125 55 35 | — — — | ns |
| Clock Pulse Width, t_W | 5 10 15 | 200 100 83 | — — — | ns |
| Clock Input Frequency, f_{CL} | 5 10 15 | dc | 1.25 2.5 3 | MHz |
| Clock Input Rise or Fall time, t_{rCL}, t_{fCL}^* | 5 10 15 | — | 15 5 5 | μs |
| Strobe Pulse Width, t_W | 5 10 15 | 200 80 70 | — — — | ns |

*If more than one unit is cascaded t_{fCL} (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.

TRUTH TABLE

| CL [▲] | Output Enable | Strobe | Data | Parallel Outputs | | Serial Outputs | |
|-----------------|---------------|--------|------|------------------|----|----------------|-----|
| | | | | Q1 | Q2 | Q3* | Q4* |
| ↘ | 0 | X | X | OC | OC | Q7 | NC |
| ↘ | 0 | X | X | OC | OC | NC | Q7 |
| ↘ | 1 | 0 | X | NC | NC | Q7 | NC |
| ↘ | 1 | 1 | 0 | 0 | 0 | Q7 | NC |
| ↘ | 1 | 1 | 1 | 1 | 1 | Q7 | NC |
| ↘ | 1 | 1 | 1 | NC | NC | NC | Q7 |

▲ = Level Change
 X = Don't Care
 NC = No Change
 OC = Open Circuit

Logic 1 \equiv High
 Logic 0 \equiv Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

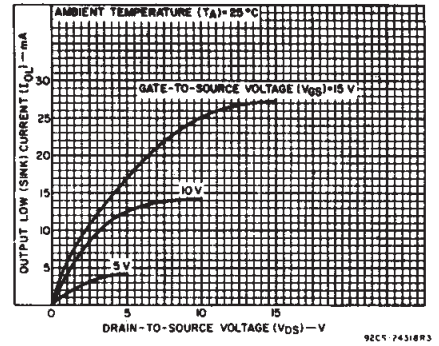


Fig. 4 — Typical output low (sink) current characteristics.

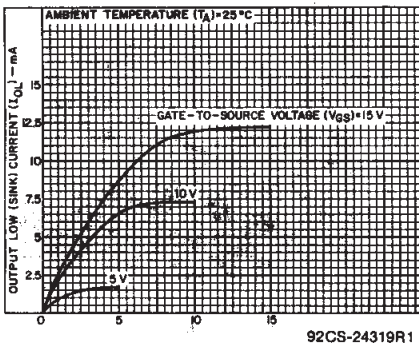


Fig. 5 — Minimum output low (sink) current characteristics.

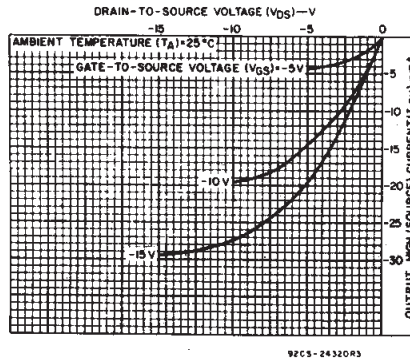


Fig. 6 — Typical output high (source) current characteristics.

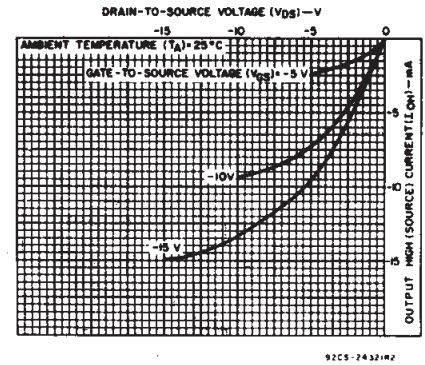


Fig. 7 — Minimum output high (source) current characteristics.

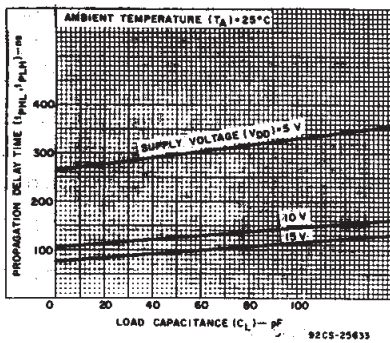


Fig. 8 — Clock-to-serial output Q_S propagation delay vs C_L .

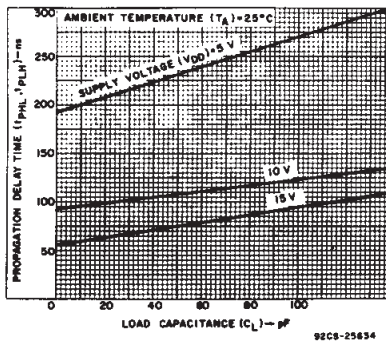


Fig. 9 — Clock-to-serial output Q_S propagation delay vs C_L .

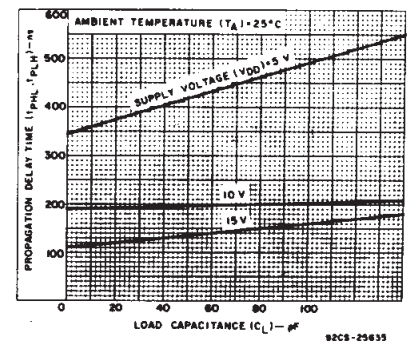


Fig. 10 — Clock-to-parallel output propagation delay vs C_L .

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 COMMERCIAL CMOS
 HIGH VOLTAGE ICs

CD4094B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0.5 | 5 | 5 | 5 | 150 | 150 | - | 0.04 | 5 | μA |
| | - | 0.10 | 10 | 10 | 10 | 300 | 300 | - | 0.04 | 10 | |
| | - | 0.15 | 15 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | |
| | - | 0.20 | 20 | 100 | 100 | 3000 | 3000 | - | 0.08 | 100 | |
| Output Low (Sink) Current, I _{OL} Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | |
| | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0.10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | |
| | 13.5 | 0.15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0.5 | 5 | 0.05 | | | | - | 0 | 0.05 | V |
| | - | 0.10 | 10 | 0.05 | | | | - | 0 | 0.05 | |
| | - | 0.15 | 15 | 0.05 | | | | - | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0.5 | 5 | 4.95 | | | | 4.95 | 5 | - | V |
| | - | 0.10 | 10 | 9.95 | | | | 9.95 | 10 | - | |
| | - | 0.15 | 15 | 14.95 | | | | 14.95 | 15 | - | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | - | 5 | 1.5 | | | | - | - | 1.5 | V |
| | 1.9 | - | 10 | 3 | | | | - | - | 3 | |
| | 1.5, 13.5 | - | 15 | 4 | | | | - | - | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | - | 5 | 3.5 | | | | 3.5 | - | - | V |
| | 1.9 | - | 10 | 7 | | | | 7 | - | - | |
| | 1.5, 13.5 | - | 15 | 11 | | | | 11 | - | - | |
| Input Current I _{IN} Max. | - | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |
| 3-State Output Leakage Current I _{OUT} Max. | 0.18 | 0.18 | 18 | ±0.4 | ±0.4 | ±12 | ±12 | - | ±10 ⁻⁴ | ±0.4 | μA |

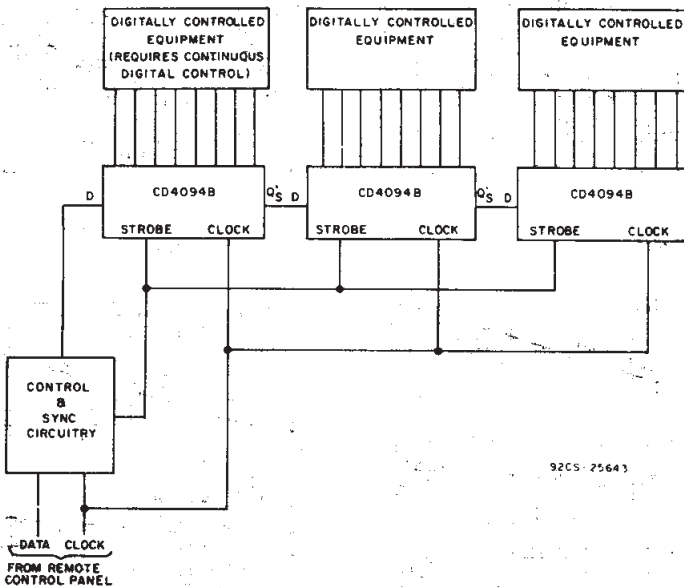


Fig. 14 - Remote control holding register.

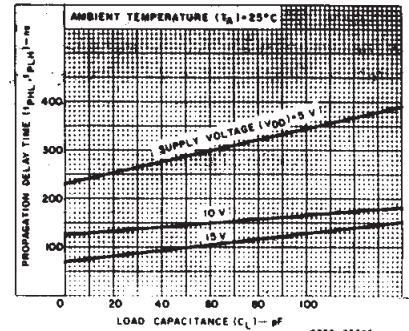


Fig. 11 - Strobe-to-parallel output propagation delay vs. C_L.

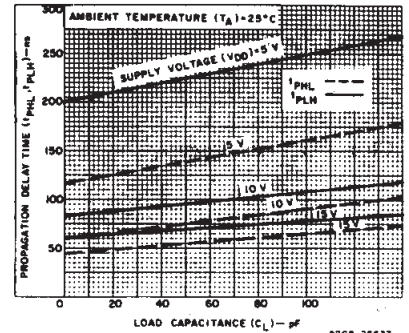


Fig. 12 - Output enable-to-parallel output propagation delay vs. C_L.

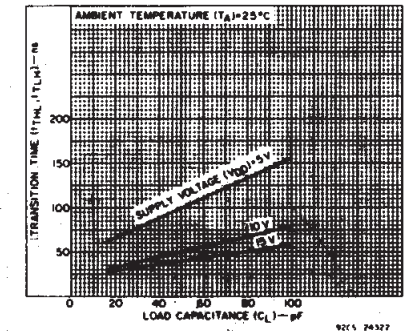


Fig. 13 - Typical transition time vs. load capacitance.

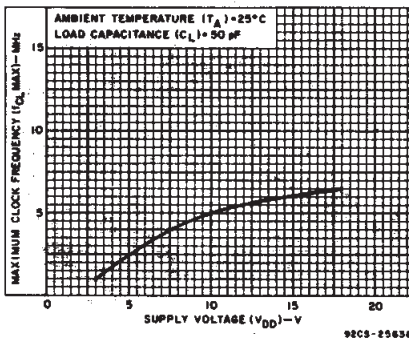


Fig. 15 - Typical maximum-clock-frequency vs. supply voltage.

CD4094B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A=25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | VDD (V) | LIMITS | | | UNITS |
|--|---------|--------|------|------|---------------|
| | | MIN. | TYP. | MAX. | |
| Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Serial Output Q_S | 5 | — | 300 | 600 | ns |
| | 10 | — | 125 | 250 | |
| | 15 | — | 95 | 190 | |
| Clock to Serial Output Q_S' | 5 | — | 230 | 460 | ns |
| | 10 | — | 110 | 220 | |
| | 15 | — | 75 | 150 | |
| Clock to Parallel Output | 5 | — | 420 | 840 | ns |
| | 10 | — | 195 | 390 | |
| | 15 | — | 135 | 270 | |
| Strobe to Parallel Output | 5 | — | 290 | 580 | ns |
| | 10 | — | 145 | 290 | |
| | 15 | — | 100 | 200 | |
| Output Enable to Parallel Output: t_{PHZ}, t_{PZH} | 5 | — | 140 | 280 | ns |
| | 10 | — | 60 | 120 | |
| | 15 | — | 45 | 90 | |
| t_{PLZ}, t_{PZL} | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Minimum Strobe Pulse Width, t_W | 5 | — | 100 | 200 | ns |
| | 10 | — | 40 | 80 | |
| | 15 | — | 35 | 70 | |
| Minimum Clock Pulse Width, t_W | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 83 | |
| Minimum Data Setup Time, t_S | 5 | — | 60 | 125 | ns |
| | 10 | — | 30 | 55 | |
| | 15 | — | 20 | 35 | |
| Transition Time; t_{THL}, t_{TLH} | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Maximum Clock Input Rise or Fall Time, t_{rCL}, t_{fCL} | 5 | 15 | — | — | μs |
| | 10 | 5 | — | — | |
| | 15 | 5 | — | — | |
| Maximum Clock Input Frequency, f_{CL} | 5 | 1.25 | 2.5 | — | MHz |
| | 10 | 2.5 | 5 | — | |
| | 15 | 3 | 6 | — | |
| Input Capacitance C_{IN} (Any Input) | — | — | 5 | 7.5 | pF |

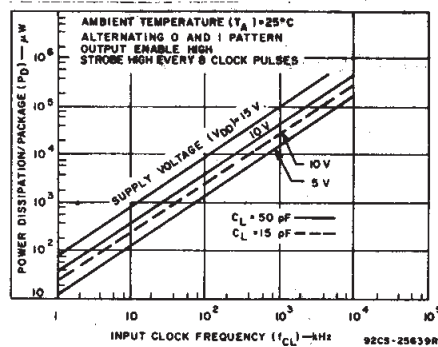


Fig. 16 — Dynamic power dissipation vs input clock frequency.

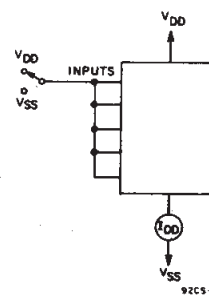


Fig. 17 — Quiescent device current test circuit.

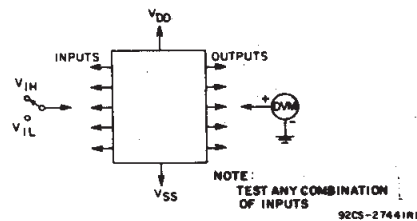


Fig. 18 — Input voltage test circuit.

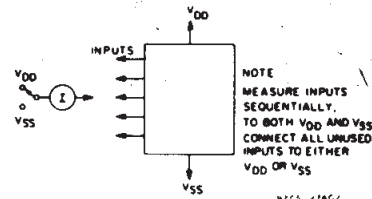
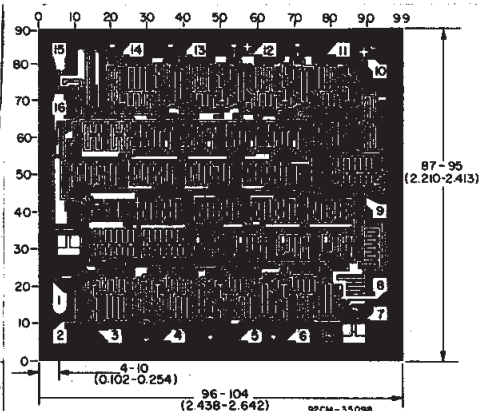


Fig. 19 — Input current test circuit.



Dimensions and Pad Layout for CD4094B Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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