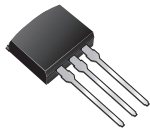


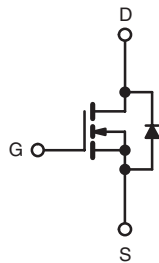
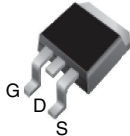
## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	900	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	8.0
$Q_g$ (Max.) (nC)	38	
$Q_{gs}$ (nC)	4.7	
$Q_{gd}$ (nC)	21	
Configuration	Single	

I<sup>2</sup>PAK (TO-262)



D<sup>2</sup>PAK (TO-263)



N-Channel MOSFET

### FEATURES

- Surface Mount (IRFBF20S/SiHFBF20S)
- Low-Profile Through-Hole (IRFBF20L/SiHFBF20L)
- Available in Tape and Reel (IRFBF20S/SiHFBF20S)
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead (Pb)-free Available



### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRFBF20L/SiHFBF20L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free	IRFBF20SPbF	IRFBF20STRLPbF <sup>a</sup>	IRFBF20STRRPbF <sup>a</sup>	IRFBF20LPbF
	SiHFBF20S-E3	SiHFBF20STL-E3 <sup>a</sup>	SiHFBF20STR-E3 <sup>a</sup>	SiHFBF20L-E3
SnPb	IRFBF20S	IRFBF20STL <sup>a</sup>	IRFBF20STR <sup>a</sup>	IRFBF20L
	SiHFBF20S-E3	SiHFBF20STL <sup>a</sup>	SiHFBF20STR <sup>a</sup>	SiHFBF20L

**Note**

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage <sup>e</sup>			$V_{DS}$	900	V
Gate-Source Voltage <sup>e</sup>			$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	$I_D$	1.7	A
		$T_C = 100$ °C		1.1	
Pulsed Drain Current <sup>a,e</sup>			$I_{DM}$	6.8	
Linear Derating Factor				0.43	W/°C
Single Pulse Avalanche Energy <sup>b,e</sup>			$E_{AS}$	180	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	1.7	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	5.4	mJ
Maximum Power Dissipation	$T_C = 25$ °C		$P_D$	54	W
	$T_A = 25$ °C			3.1	
Peak Diode Recovery dV/dt <sup>c,e</sup>			dV/dt	1.5	V/ns

\* Pb containing terminations are not RoHS compliant, exemptions may apply

# IRFBF20S, IRFBF20L, SiHFBF20S, SiHFBF20L



Vishay Siliconix

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	N

## Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ ; starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 117\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 1.7\text{ A}$  (see fig. 12).
- $I_{SD} \leq 1.7\text{ A}$ ,  $di/dt \leq 70\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- Uses IRFBF20/SiHFBF20 data and test conditions.

<b>THERMAL RESISTANCE RATINGS</b>				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case	$R_{thJC}$	-	2.3	

## Note

- When mounted on 1" square PCB (FR-4 or G-10 material).

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		900	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	1.1	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 900\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	100	$\mu\text{A}$
		$V_{DS} = 720\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.0\text{ A}^b$	-	-	8.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 1.0\text{ A}^b$		0.6	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	490	-	pF
Output Capacitance	$C_{oss}$			-	55	-	
Reverse Transfer Capacitance	$C_{riss}$			-	18	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 1.7\text{ A}$ , $V_{DS} = 360\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	38	nC
Gate-Source Charge	$Q_{gs}$			-	-	4.7	
Gate-Drain Charge	$Q_{gd}$			-	-	21	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 450\text{ V}$ , $I_D = 1.7\text{ A}$ , $R_G = 18\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ , see fig. 10 <sup>b</sup>		-	8.0	-	ns
Rise Time	$t_r$			-	21	-	
Turn-Off Delay Time	$t_{d(off)}$			-	56	-	
Fall Time	$t_f$			-	32	-	

<b>SPECIFICATIONS</b> $T_J = 25^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	1.7	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	6.8	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = 1.7\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = 1.7\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	350	530	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	0.85	1.3	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c. Uses IRFBF20/SiHFBF20 data and test conditions.

**TYPICAL CHARACTERISTICS**  $25^\circ\text{C}$ , unless otherwise noted

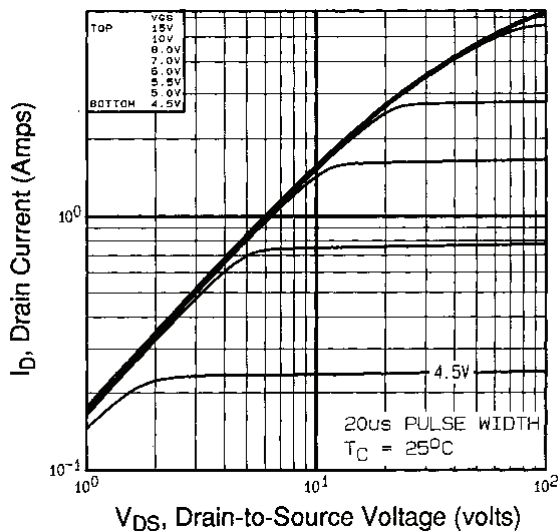


Fig. 1 - Typical Output Characteristics

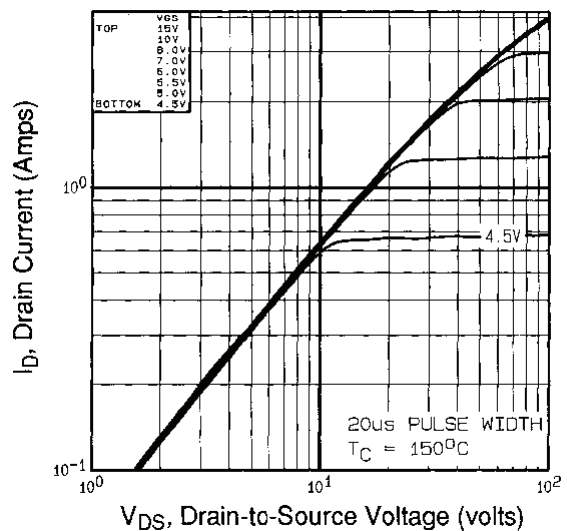


Fig. 2 - Typical Output Characteristics

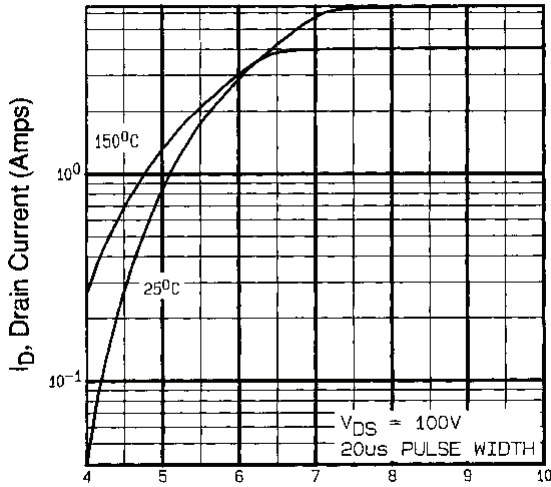


Fig. 3 - Typical Transfer Characteristics

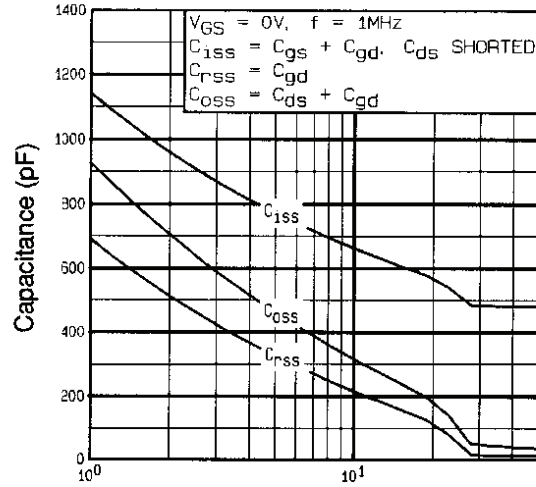


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

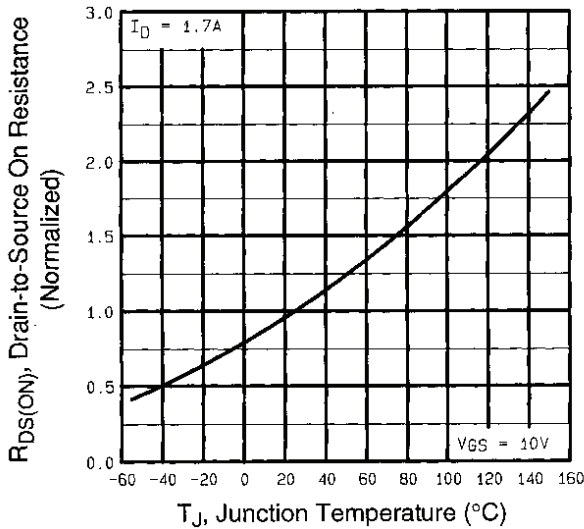


Fig. 4 - Normalized On-Resistance vs. Temperature

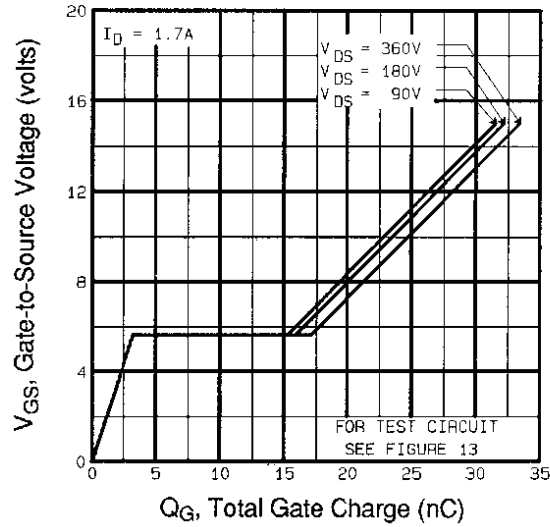


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

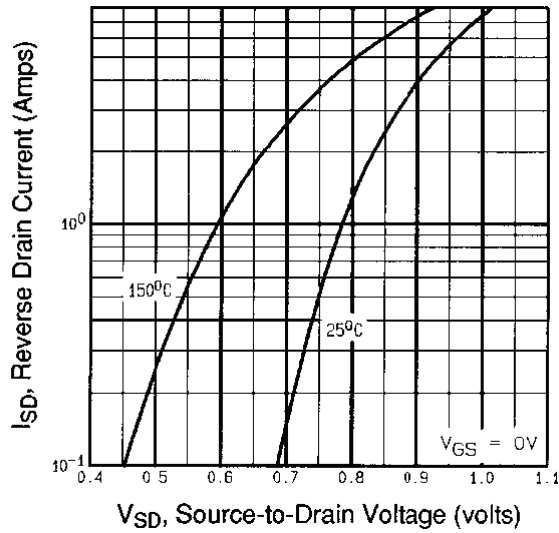


Fig. 7 - Typical Source-Drain Diode Forward Voltage

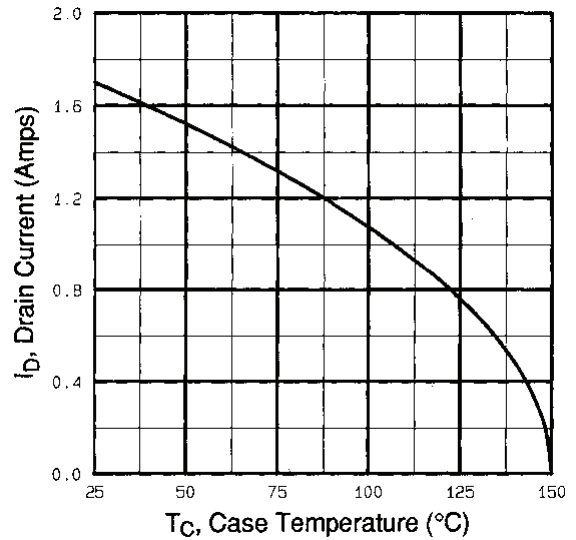


Fig. 9 - Maximum Drain Current vs. Case Temperature

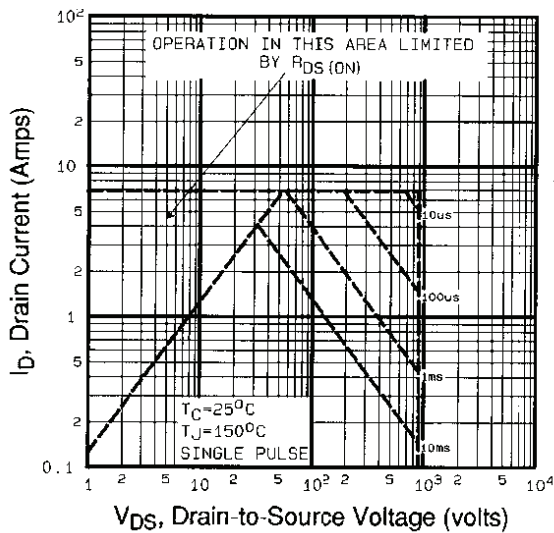


Fig. 8 - Maximum Safe Operating Area

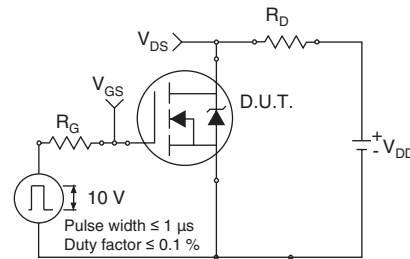


Fig. 10a - Switching Time Test Circuit

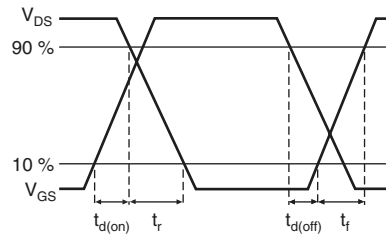


Fig. 10b - Switching Time Waveforms

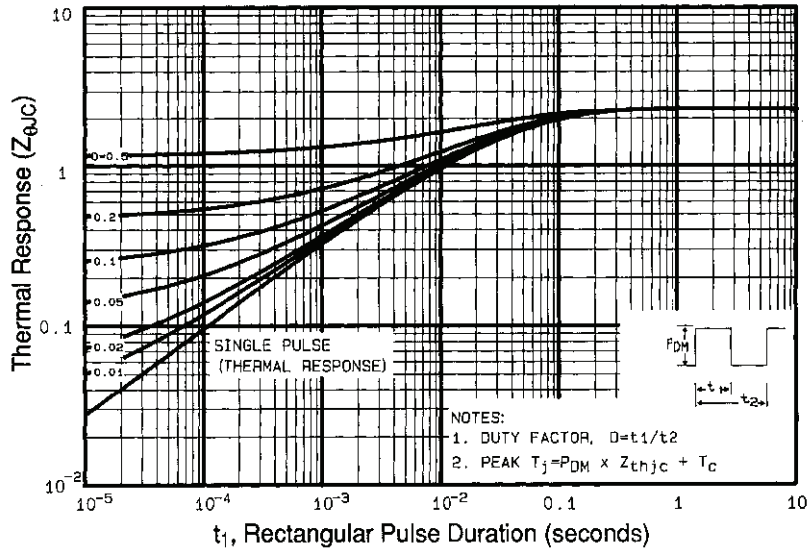


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

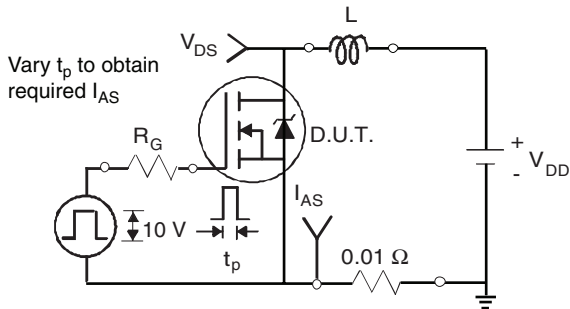


Fig. 12a - Unclamped Inductive Test Circuit

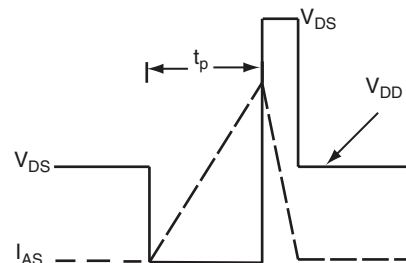


Fig. 12b - Unclamped Inductive Waveforms

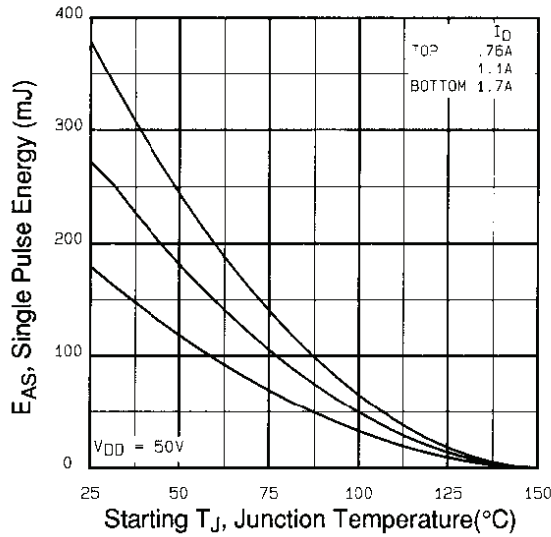


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

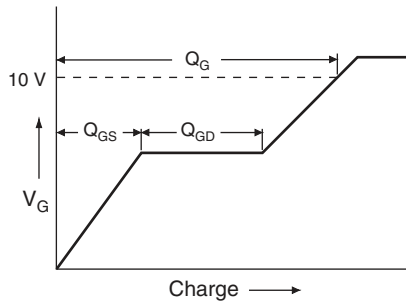


Fig. 13a - Basic Gate Charge Waveform

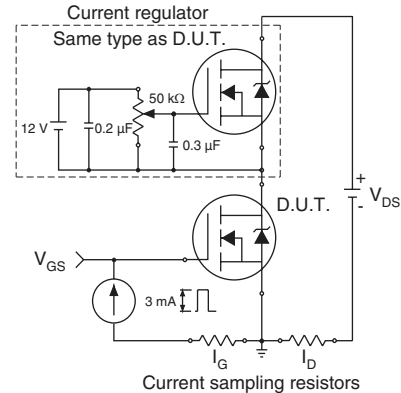
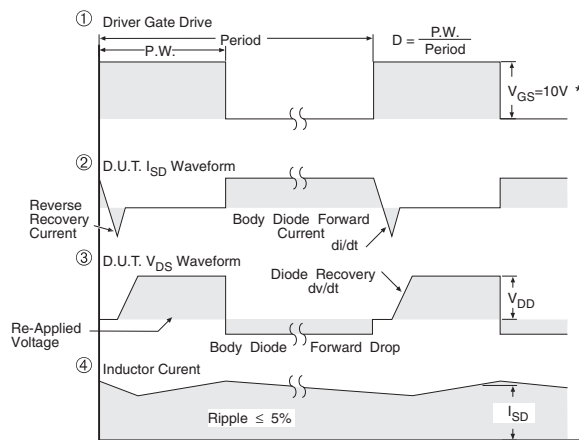
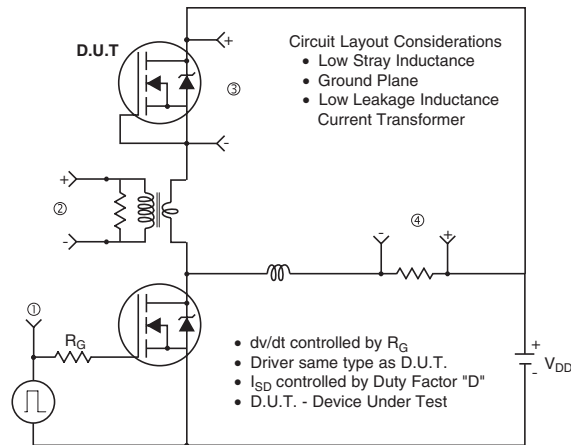


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

Fig. 14 - For N-Channel

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